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Sub-nanometer Displacement Sensing for the Nanogate – A Tunable Nanometer Gap

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Abstract

We have developed a sub-nanometer level displacement sensing system for a MEMS device called the Nanogate. The Nanogate is a tunable nanometer gap between ultra smooth surfaces of silicon and Pyrex. The separation between the surfaces can be as small as a few nanometers to as large as one micron. The Nanogate was created as a valve for precisely controlling very small gas and liquid flows, but it is also envisioned as a device where the variable gap can be used to filter particles and molecules by size. One advantage of our system is that the displacement measurement does not directly measure the capacitance of the nanometer gap hence does not depend on the dielectric properties of the material flowing in the gap. Our results show our capacitive sensor with a noise floor of 1.2Å RMS and long-term drift of 2.5nm.

Keywords

Capacitive sensing, nanoscale sensing, MEMS, BioMEMS, Microfluidics, Nanogate

INTRODUCTION

The Nanogate [1] is a micro electromechanical systems (MEMS) device capable of accurately and repeatably controlling the separation of a nanometer gap between two ultra-flat, mating surfaces of silicon and Pyrex wafers. The nanometer gap is controlled using a lever-fulcrum structure made by micromachining the silicon diaphragm and then selectively bonding it to a drilled Pyrex wafer. The separation distance between the silicon and Pyrex wafers can range from a few nanometers to a micron, while the aspect ratio between the lateral dimension and the separation of the gap can be as large as 10^6.

The Nanogate was created as a building-block for nanofluidics where precise control of gas and liquid flow is required [2, 3, 4]. The variable nanometer gap has also been envisioned as a mechanical filter for nano-particles and molecules, taking advantage of the large aspect ratio between its lateral and vertical dimensions. To create an experimental system to test this hypothesis, the Nanogate needed a sensor system to measure gap displacement with extreme precision and stability. Capacitance sensors have been developed to measure displacement with great accuracy [5, 6, 7] and have been integrated into MEMS systems such as the Analog Devices accelerometers [8]. The challenge of this research is to develop a system that is compatible with microfluidics experiments in the Nanogate. This paper describes the development of a capacitive sensor for the Nanogate including the sensor design, fabrica-

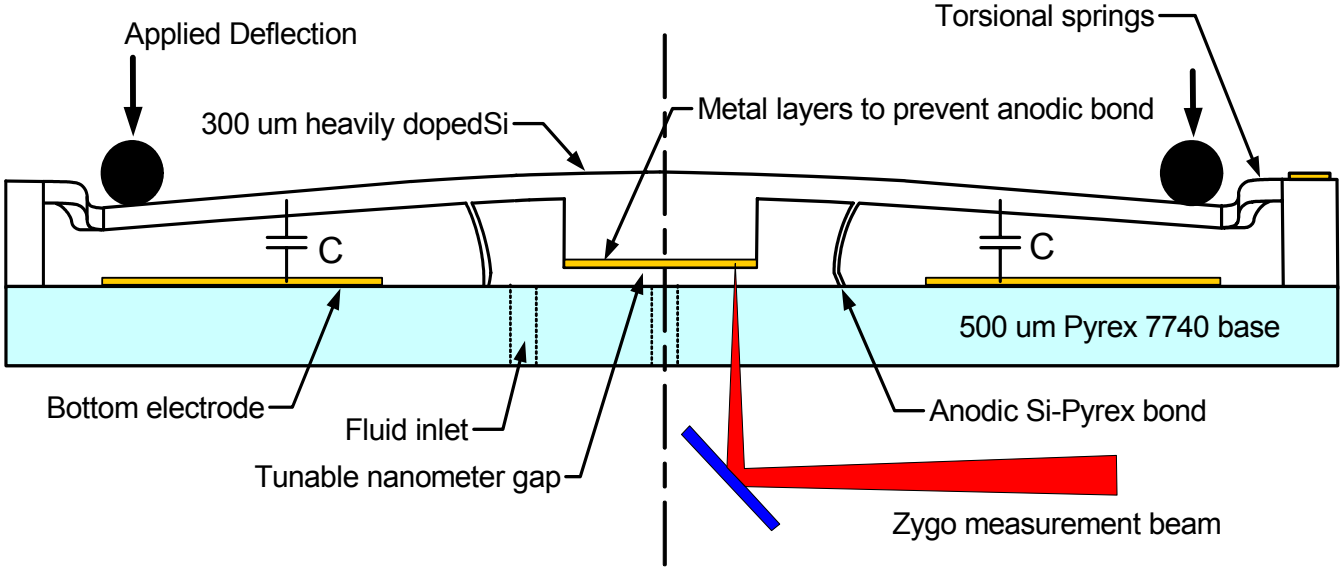

Figure 1. Schematic Cross section of the nanogate

tion process, circuits for capacitive sensing, and results.

The silicon-Pyrex structure of the Nanogate is shown conceptually in Figure 1 where the axis of revolution is through the center of the device. Figure 2 shows a 3D CAD model of this structure. At the center of the diaphragm is a 1.5mm diameter valveland region, where the smooth silicon surface rests in intimate contact with a smooth Pyrex glass surface. The roughness of this region varies depending on the quality of silicon wafers, which may be better than 3Å RMS. An SEM of this region is shown in figure 3.

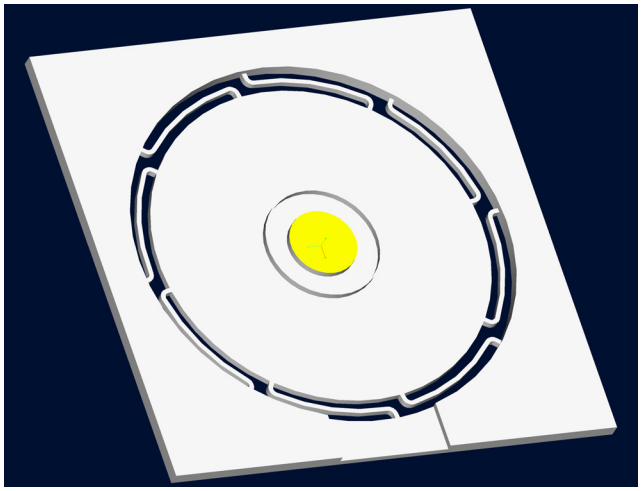

Figure 2. CAD model of the nanogate silicon diaphragm

Concentric with the valveland is a ring protrusion (fulcrum) measuring 15µm thick, 150µm tall and 2.25mm in diameter. This ring is anodically bonded to the Pyrex glass diaphragm to form a circular fulcrum such that when the outside edge of the silicon diaphragm is deflected, the silicon valveland is pried apart from its complementary glass surface, creating a tunable gap. The outer diameter of the silicon diaphragm is 7.5mm, resulting in an approximate mechanical transmission ratio of 16:1. The displacement reduction from outside edge to valveland acts as a mechanical transmission, and magnifies the mechanical impedance and increases the displacement precision of the central valveland. The fulcrum structure reaches its maximum designed strain when the valveland is opened approximately 1µm, implying that maximum travel of the outer edge is 15µm. Around the outside of the silicon diaphragm are flexible torsional springs (Figure 2) that holds the diaphragm in place during the fabrication processing.

SENSOR DESIGN

In previous work on the Nanogate [2, 3], the valveland displacement was determined with a Zygo ZMI-1000 single point optical probe. The Zygo is a Michelson interferometer that uses the optical phase difference between a probe beam and a reference beam to measure displacements with a resolution of 2.5nm. In our setup, the probe beam is focused down to a 0.3mm spot and reflected off the valveland through the Pyrex bottom. Although the Zygo's resolution is extremely good, the non-differential nature of this measurement makes it prone to errors from mechanical and thermal drift in the Nanogate fixture. These errors can accumulate to over 100nm over a few hours. Consequently, a capacitance based measurement system, measuring only a differential displacement could potentially provide much better resolution.

The functional requirements of the capacitive sensor include the following: displacement measurement of the central region with accuracy better than 1nm; the electrical properties of the sensor must not interfere with or be dependent on the liquid or gas flow in the gap; the sensor electrodes must be tolerant to variations in the Nanogate fabrication process; and the sensor electronics must be mechanically integrated with the Nanogate die and its external actuator.

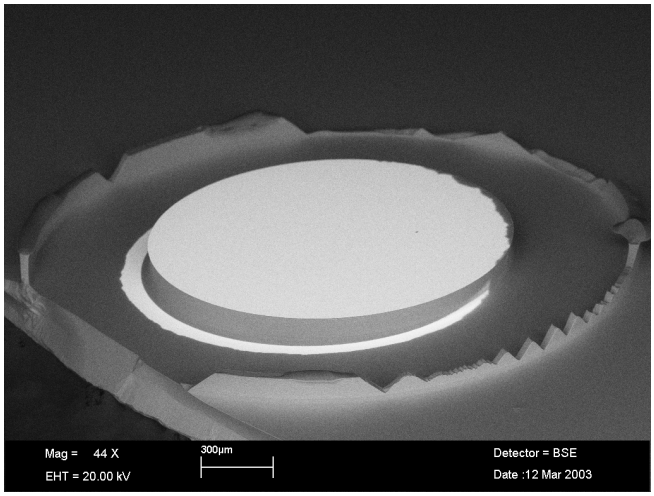

Figure 3. SEM of nanogate valveland with (deliberately) broken fulcrum

The most straightforward approach to the Nanogate displacement would have been to put electrodes on either side of the gap. However, depending on the dielectric and conductive properties of the liquid or gas in the gap, the impedance measured across the Nanogate could vary greatly. To avoid this problem, the capacitive measurement is made at the outside edge of the cantilever with the silicon diaphragm as one electrode and a gold trace deposited on Pyrex as the other electrode. It is assumed that the deflection around the outside edge maps exactly to movement of the center and do not change over time because a silicon wafer is essentially a single crystal and has no mechanism for creep. However, the exact mapping of the outer edge deflection to center deflection on the silicon diaphragm cannot be exactly predicted a priori because of MEMS fabrication variations in the size of the fulcrum and strength of the anodic bond. Therefore, it is necessary to calibrate the capacitance value as a function of actual gap displacement found using the Zygo. Furthermore, by calibrating in a rela-

tively short time, it is possible to avoid the long-term drift errors of the Zygo.

To a first order approximation, the capacitance between the outer edge of the silicon diaphragm and gold trace on the Pyrex die can be modeled as a parallel plate capacitor, such that

$$C = \frac{\varepsilon_0 A}{d}, \quad (1)$$

where A is the area of the electrodes, d is the spacing of the electrodes, and ε_0 is the permittivity of free space. For small plate deflections, the capacitance varies as,

$$C = \frac{\varepsilon_0 A}{d_0} - \frac{\varepsilon_0 A}{d_0^{\,2}} \Delta d \,, \quad (2)$$

where d_0 is the initial undeflected distance and Δd is the displacement caused by the external deflection.

The initial separation of the plates is approximately 150 um with a total expected travel of 15µm. This means that the capacitance will vary up to 10% of the value at the undeflected state. The total area of the electrode pattern is approximately 24.5mm^2, resulting in a undeflected capacitance of approximately 1.45pF. With a target of better than 1 nm resolution at the center, it is necessary to measure capacitance with accuracy better than 0.3fF or a signal-to-noise ratio of 74dB.

The resolution of this capacitive sensor will be limited by noise and drift. Noise is an innate parameter of electronic devices and it is rooted in the random thermal motion of the electrons as well as imperfections in semiconductor devices. Drift is a low frequency phenomenon primarily caused by thermal fluctuations within the system. By using synchronous detection [5] with appropriate components, both noise and drift in the electronics can be minimized. Synchronous detection involves mixing a signal of interest with a reference signal of the same frequency and phase. As a result the desired signal is mixed down to DC while out of band noise, particularly those previously at DC, can be filtered out.

FABRICATION

The Nanogate is fabricated using conventional MEMS fabrication tools at MIT's Microsystems Technology Laboratory. The simplified fabrication process is shown in figure 4. The process starts with 4 inch, 300µm thick, double side polished, low resistivity silicon wafers. A 1µm thick sacrificial layer of SiO_2 is grown thermally and patterned using BOE with positive photoresist as a mask layer. The topside of the silicon wafer is then etched using DRIE to a nominal depth of 150µm. The same lithography steps are repeated for the bottom side of the silicon wafer with 150µm deep DRIE to produce the lever-fulcrum structure. The next step is to metallize the valveland surface to prevent anodic bonding in that area. Four layers of metals Ti, Pt, Ti, and Au are deposited using an e-beam sputter at thicknesses of 20, 100, 20, 100nm respectively. The Ti layers act as adhesion layers, while the Au layer deters oxidation of the silicon and hence the anodic bond. The Pt layer acts as a diffusion barrier to prevent the formation of Au-Si eutectic during the thermal cycle of the anodic bond. Finally, the topside of the silicon wafer is also metallized with Ti-Au to act as a backside electrical contact.

The bottom electrode of the capacitor is deposited on Pyrex glass using a lift-off process. Positive photoresist is spin-coated onto the Pyrex glass and patterned using photolithography. Metal layers of Ti and Au are deposited by e-beam evaporation and lift-off is performed in acetone. After solvent and DI-water clean, the Pyrex and silicon wafers are anodically bonded at 800V and 350ºC. Finally, each 20x20mm Nanogate die is separated from the wafer using a diesaw.

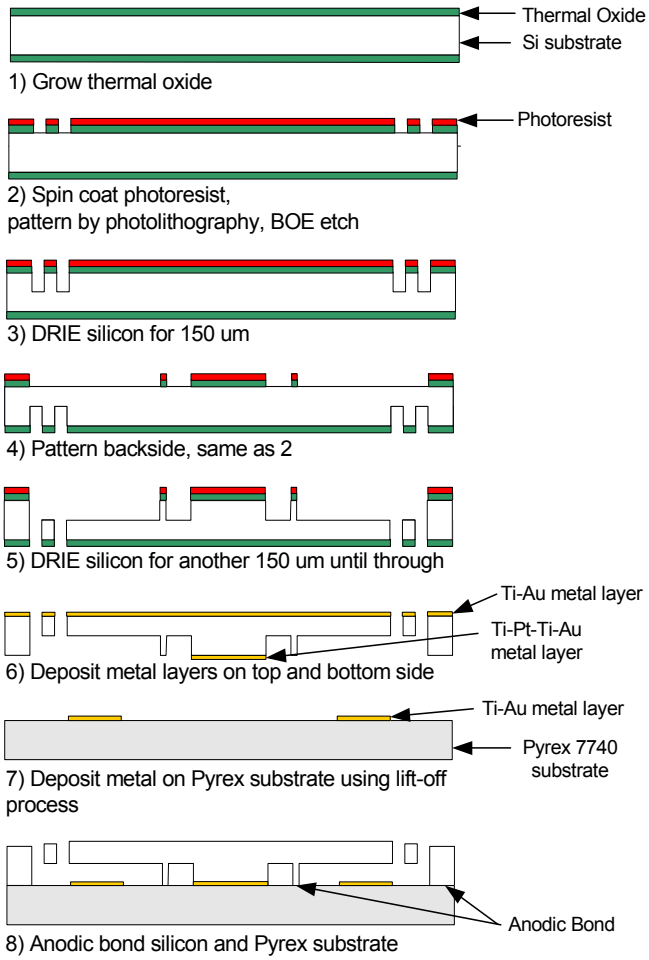

Figure 4. Simplified fabrication process of the Nanogate

Wire contact between the electrodes and the capacitive sensing printed circuit board are made using a single strand of wire from 26AWG stranded wire. The wires are silver epoxy glued to the Ti-Au electrical traces on the Nanogate and soldered to the printed circuit board.

The Nanogate is actuated externally with a Picomotor 8701 piezoelectric lead screw actuator from Newfocus [8]. The Picomotor is preloaded with a flexure and pushes on the outer edge of the Nanogate via a rubber O-ring. In order to mechanically fixture the Nanogate, each die is bonded to a 1"x1"x¼" Pyrex substrate using a leak sealant epoxy [10]. The Pyrex substrate is then clamped into a metal fixture, which integrates with the capacitive sensing circuit board and aligns the Zygo probe beam. The metal fixture is made of Super Invar, a material designed with the least thermal expansion coefficient at room temperature.

CIRCUITS FOR CAPACITIVE SENSING

The capacitive sensing scheme in the Nanogate can be conceptually divided into four parts: front-end amplifier, demodulator, output filter / signal conditioner, and data acquisition system (Figure 5).

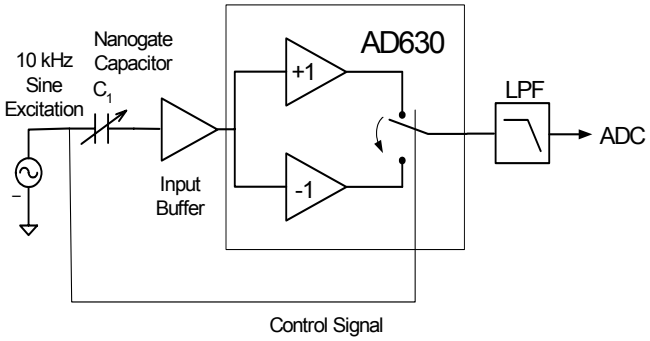

Figure 5. Conceptual schematic of the Nanogate capacitive sensor

The front-end amplifier is designed to detect current through the Nanogate capacitor with the least amount of signal degradation from parasitic capacitance, amplifier input bias current, and noise. A low-impedance, transimpedance configuration was chosen because the input pin is at a virtual ground, which makes it immune to parasitic capacitance to ground. The OPA129 [11] operational amplifier from Burr-Brown was chosen because it is specified for an extremely low input bias current of 100fA maximum. The OPA129 is also specified for extremely low noise at 15nV/$\sqrt{Hz}$ voltage and 0.1fA/$\sqrt{Hz}$ current noise at 10 kHz.

The front-end amplifier circuit is shown in Figure 6. The Nanogate capacitor is represented by C_1 and excited with a 10kHz sine wave from an Agilent 33120A function generator. The current through C_1 is converted to a voltage through a reference capacitor, C_2 such that

$$V_{out} = \frac{C_1}{C_2},$$

as long as the time constant of the feedback loop is much greater than the excitation frequency. The resistive network of R_1, R_2, and R_3 is necessary to provide a high impedance DC path to ensure that the inverting input does not float to arbitrary voltages. Using the T-configuration in the feedback loop serves to magnify the effective resistance across C_2 to 500MΩ, beyond what is ordinarily possible with conventional components. C_2 is chosen to be approximately the same as C_1 and the resulting time constant of the feedback loop is approximately 100Hz.

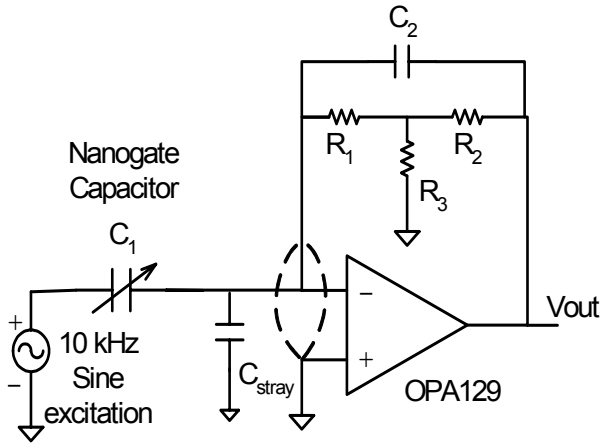

Figure 6. Front-end transimpedance amplifier circuit

The AD630 synchronous demodulator from Analog Devices [12] follows the input buffer in the signal chain. The AD630 has two parallel input amplifiers setup with gains of +1 and a –1. A synchronization signal of the same frequency and phase of the input signal triggers a channel switch at the zero crossing with the effect of mixing the input signal to a square wave of the same frequency and phase. As a result, the desired 10kHz is mixed down to DC, while the 1/f and white noise are mixed out to higher frequencies.

Signal from the synchronous demodulator is filtered to recover the necessary DC information and level shifted to fall within range of the 0-5V range of the ADC. A six-pole voltage-controlled voltage-source low pass filter [13, 14] with a roll-off frequency at 100Hz was designed for this task using low-noise LT1793 operational amplifiers [15]. The level shifter also uses a LT1793 amplifier with a LT1019 bandgap reference [16] to set the reference voltage.

The data acquisition system includes a precision 24-bit ADC, a microprocessor that relays data from the ADC, and software on a PC to collect and store the data. The LTC2440 from Linear Technologies [17] is used to digitize the capacitive sensing data. The LTC2440 is a differential 24-bit sigma-delta A/D with a variable sampling rate. It is capable of detecting 19 bits of effective resolution at 1 kilo-samples-per-second. The converter interfaces via a MSP430F149 microprocessor from Texas Instruments. The microprocessor also controls the motion of the Picomotor actuator. The digitized signal is transmitted via a RS-232 line to a PC. Software written in Visual Basic stores and

graphs three streams of data from the capacitive sensor, Zygo interferometer, and actuator.

RESULTS AND DISCUSSION

The graph of Zygo measured displacement versus capacitance graph has three distinct regions (Figure 7). In region I, the capacitance is increasing in response to the deflection from the actuator while the central valveland remains fixed. This is because the deflection of the outer edge must first overcome the preload due to the additional material of the metal film layer. Region III shows the valveland displacement varying as a linear function of capacitance as in equation (2). Region II is the non-linear, transition between regions I and III. It is hypothesized that this transition region is caused by asymmetry in the actuation of the outer edge of the silicon diaphragm and with better actuation schemes the rounded region can be reduced. The roundedness of this region makes it difficult to define a zero point. It is possible to interpolate this point by fitting a straight line to region III in Figure 7 and finding its intercept with the mean of region I.

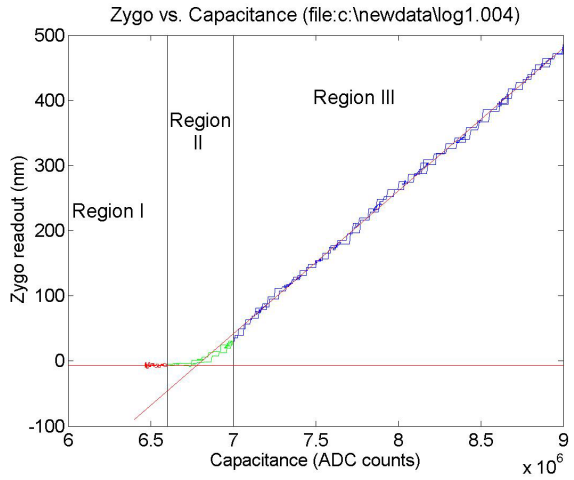

Figure 7: Zygo vs. Capacitance divided into 3 regions

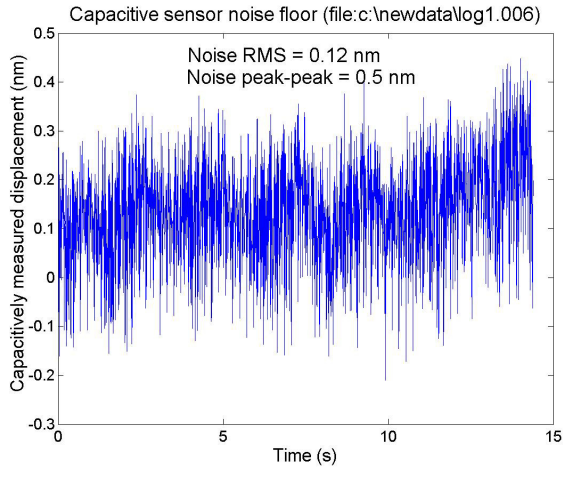

Figure 8: Capacitance short-term baseline

Figure 8 shows the noise floor of the capacitive measurement. The ADC value is converted to nanometers of displacement from the slope obtained in region III of Figure 7. The RMS variation is approximately 1.2Å with a peak-to-peak variation of approximately 5Å, or equivalent to 160μV and 660μV respectively. The ADC and output filters have a measured baseline of 50μV, which means that the rest of the noise originates from phase jitter in the demodulator or from electronic and acoustic pickup in the Nanogate capacitor.

Figure 9 shows the slow drift of the output over 4 hours. The peak-to-peak variation is 2.5nm, or equivalently, 3.3mV. The mechanisms for this error include slow variations in excitation amplitude from the function generator and thermal fluctuations in the output filter and ADC.

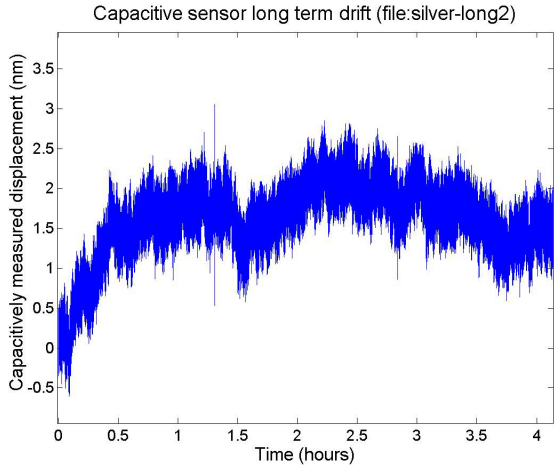

Figure 9: Capacitance value drift over 4 hours

CONCLUSION

We have developed a sub-nanometer capacitive sensing system for the Nanogate, a tunable nanometer gap between two polished surfaces of silicon and Pyrex. Our system obtained a baseline resolution of 1.2Å RMS and a long-term drift of 2.5nm. This system uses the uses outside edge of the Nanogate to sense displacement and is therefore compatible with micro and nanofluidic applications where material is passed through the gap. Future work will include reducing long-term drift error, improving the actuator assembly, and using quadrant electrodes to measure uneven deflections.

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REFERENCES

[1] Slocum, A. H. “Method of and apparatus for substance processing with small opening gates actuated and controlled by large displacement members having fine surface finishing.” US Patent #5,964,242. 1999.

[2] White, J., Ma, H., Lang, J., Slocum, A. “An instrument to control parallel plate separation for nanoscale flow control,” *Review of Scientific Instruments*, vol. 74, number 11, Nov. 2003.

[3] Ma, H. and White, J. Packaging and Initial Characterization of the Nanogate. MIT. MAS.962 Final project report. 2001.

[4] White, J. “Nanoscale Flow Control”, Ph.D. thesis, MIT, 2003.

[5] Baxter, L. K., *Capacitive Sensors - Design and Applications,* IEEE Press, 1997.

[6] Paradiso, J.A., “New technologies for monitoring the precision alignment of large detector systems”, Nuclear Instruments and Methods in Physics Research A, vol. 386, pp. 409-420, 1997.

[7] Puers, B., "Capacitive sensors: when and how to use them," *Sensors and Actuators*, vol. A37-A38 pp. 93-105, 1993.

[8] Analog Devices MEMS accelerometers: http://www.analog.com/

[9] Newfocus 8701 Picomotor datasheet: http://www.newfocus.com/Manuals/8X01_Manual_RevH.pdf

[10] Kurt Lesker KL-5, Kurt Lesker Inc., Clarton, PA

[11] OPA129 datasheet: http://www.ti.com/

[12] AD630 datasheet: http://www.analog.com/

[13] Lancaster, D., *Active Filter Cookbook*, 2nd Ed. Newnes, 1996.

[14] Horowitz, P. and Hill, W. *The Art of Electronics,* 2nd Ed. Cambridge University Press, 1989.

[15] LT1793 datasheet: http://www.linear.com/prod/datasheet.html?datasheet=504

[16] LT1019 datasheet: http://www.linear.com/prod/datasheet.html?datasheet=95

[17] LT2440 datasheet: http://www.linear.com/prod/datasheet.html?datasheet=900