Embedded Low-Power Wireless Sensor System: Design of a Software Radio Base Station

by
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Bachelor of Science in Electrical
Engineering and Computer Science,
Massachusetts Institute of Technology, 1998

Submitted to the Department of Electrical Engineering and Computer Science

in Partial Fulfillment of the Requirements for the Degree of

Master of Engineering in Electrical Engineering and Computer Science

at the Massachusetts Institute of Technology

April 6, 2001

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ABSTRACT

This research proposes an implementation of a base station for a wireless sensor system for use at the MIT Media Lab and beyond. The goal is to create a wireless network employing low-power, scalable, reconfigurable chipset designs. This network will become the backbone of a multitude of sensor projects. Software radios are a key necessity for such a network to be realized.

The design of this network requires several stages. This thesis addresses the first stage: implementing a one-way wireless link between a transmitter and base station. The primary consideration for the design is minimizing the bit error rate. The transmitter has two integrated circuit chips developed by Charles Sodini's group at MIT's Microsystems Technology Laboratories. The base station, drawing on the concepts developed within emerging field of "Software Defined Radio," consists of a radio frequency board and a digital board. The RF board receives a 1.89 GHz, Gaussian frequency shift keyed modulated signal at 2.5 Mbps. The received signal is modulated down to 140 MHz and then digitized. The demodulation and clock recovery are performed in the digital domain using a field programmable logic array.

Thesis Supervisor: Joseph A. Paradiso
Title: Principal Research Scientist, MIT Media Lab

ACKNOWLEDGMENTS

Many thanks to Joe Paradiso, for his continued support and encouragement through this three year adventure. This project would not have been possible without you.

Thank you to the Media Lab providing the means and space to learn and grow.

To, Charlie Sodini, Jim McArthur, Ketan Peta,l for teaching me how to both ask clear questions and find the answers.

To Anantha Chandrakasan and all his students, for providing a welcoming and stimulating atmosphere early on in my graduate career, and to the students at PHM, Neil and Shri for renewing my energy and enthusiasm for circuit design at the conclusion of this chapter of graduate school.

Special thanks to Dan McMahill, Don Hitko, Manish Bhardwaj and Wendi Heinzelman for being both knowledgeable and willing to answer various technical questions.

Thanks to ALL the application engineers at the different companies I have called over the past three years, the phone calls and email exchanges have become my "office hours" for graduate school.

Rich Goldhammer, thank you for all your weekly coaching meetings and helping me become aware of the academic skills I have developed and for teaching me new skills.

Thank you, Amy, Jessica, and Barbara, for caring about the human side of Zoe.

Anne Pollock, I have such deep respect for your determination, thank you for teaching me how to persevere when the going gets tough. I hope some day we can renew our friendship.

Jenn Weeber, thank you for never judging me.

To Saul and Jeff, thank you for both encouraging and allowing me to be Zanny Zoe.

Charlie Camp, thank you for always believing in me, and teaching me life survival skills.

To Susan and the MIT women's crew team, thank you for teaching me discipline, perseverance, and importance of a team.

To the Ballroom Dancing Team, thank you for renewing my love of dance.

To Cecile, thank you, for awakening my creativity and teaching me the importance and joys of a home.

To Bobby, Ciccio, Pino, Chouch, Pouch, Biloo, George, Flatty, Grumpy and Baboo, thank you for never questioning my reasons and always being at my side whenever I needed you.

To my writing saviors, Amy Banzaert and Justine Cassell, the thesis write-up would not be possible with your encouragement, thank you. You both have taught me the meaning of real friendship.

Thank you to both of my proof readers, Nisha Checka and Stacy Morris.

To Barb and Terrie, thank you for guiding me through these years and each helping me in your own way.

Mom, thank you for your love and encouragement, you are the one that taught me anything is possible if I set my mind to it. I enjoyed sharing the ups and downs with you as we both worked on our graduate degrees. Congratulations on your MBA and Capital Campaign.

Papa, thank you for your love and support, you are one that helped trained my mathematical mind from day one and taught me a strong work ethic.

I want to thank myself for putting up with myself, for being courageous to take on challenging problems and find the necessary support, both external and internal.

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LIST OF TERMS AND ABBREVIATIONS

Abreviation or Term	Description	Equation
ADC	Analog to Digital Converter	
AGND	Analog Ground	
BER	Bit Error Rate	
BPF	Band Pass Filter	
dBc	Decibles relative to the carrier frequency	
dBi	Decibles relative to one unit interval [1]	
dBm	The term dBm simply means how many dB something is above/below 1mW. While dB is just a ratio, dBm refers to a power measurement.	$y_{dBm} := 10 \cdot \log\left(\frac{x_{mW}}{1\ mW}\right)$ $x_{mW} := 1\ mW \cdot \left(10^{\frac{y_{dBm}}{10}}\right)$
DECT	Digital Enhanced Cordless Telecommunications	
DGND	Digital Ground	
GSM	Global System for Mobile communications	
HF	High Frequency	
IF	Intermediate Frequency	
IIP3	Input refered 3rd Inctercept point	
IM	InterModulation	
IMD	InterModulation Distortion	
ISI	InnerSymbol Interference	
LF	Low Frequeny	
LNA	Low Noise Amplfier	
LO	Local Oscillator	
LPF	Low Pass Filter	
RF	Radio Frequency	
RMS	Root Mean Squared	
SAW	Surface Acustic Wave	
SDR	Software Defined Radio	
SFDR	Spurious Free Dynamic Range	
SINAD	Signal-Noise-distortion to noise-Distortion ratio	
SMA	SubMinature type A connector	
SNR	Signal to Noise Ratio	
VCO	Voltage Controlled Oscillator	

1 Introduction

1.1 Motivation for Software Defined Radios

Almost daily, a new wireless device is introduced into the marketplace. Few worldwide standards exist; in fact, virtually every type of device has its own protocol. New protocols and modulation schemes are constantly being developed, adding to the multitude of protocols on the market today.

Companies that produce base stations cannot afford to change the base station hardware each time they need an upgrade. It would be far more efficient to download a new protocol to a reconfigurable base station. Optimally, companies would have completely reconfigurable base stations, allowing them to switch to any frequency spectrum without changing the hardware ever.

There is a critical need for base stations that are reconfigurable and can thereby adapt to new protocols. The ideal device consists of a very wide band antenna, a fast analog-to-digital converter (ADC), and an extremely fast parallel processing application specific integrated circuit (ASIC). Unfortunately, such a device has not yet been developed. This project explores the current technological limits, physical limits, and mathematical principles that restrict the implementation of a reconfigurable base station. Figure 1 illustrates the desired wireless network, including multiple sensors in a two way link with a software radio base station. After examining the theoretical and practical limitations of building a software radio base station, including availability of materials in today's market, this project suggests and develops a prototype for an intermediate frequency (IF) sampling receiver.

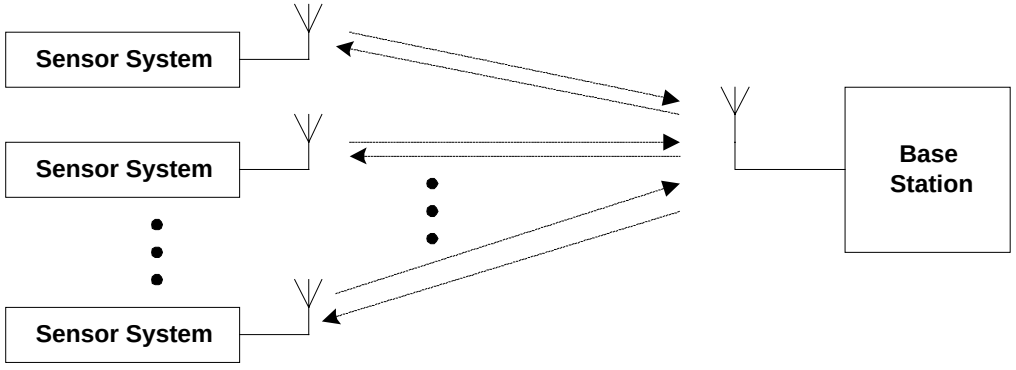


Figure 1. Block diagram illustrating the desired network.

1.2 Project Approach

This document provides a tutorial on SDR principles, constraints, and resources . The overall project approach is diagrammed in Figure 2. The project approach first involves researching the architecture of traditional base stations and then understanding how and why software defined radios (SDR) alter the traditional model. Papers on theoretical SDR present constraints that are stricter than what is commercially available [3-6]. This limitation forced a closer review of the theories that produced the constraints presented in the literature. The results of this research clarified which constraints were excessive and established which trade-offs were feasible, when implementing a SDR.

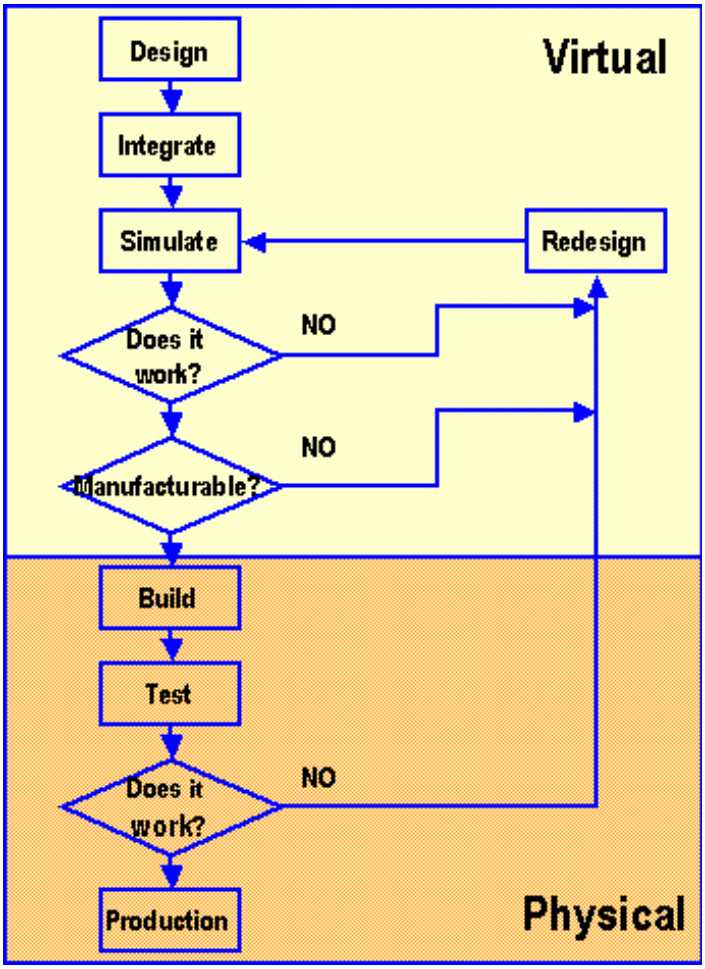


Figure 2. Block diagram of the design process [2].

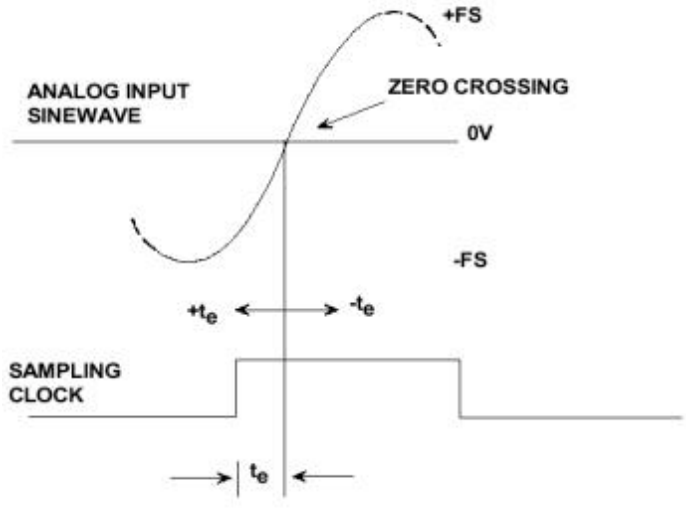


Figure 3. Jitter is when the sampling clock edge's location changes over time [8, see pg 4-29].

The concept of sampling clock jitter is detailed in chapter 7, for now, Figure 3 illustrates the basic idea. A clock with 1ps jitter means that the clock edge's location in time only varies by 1ps. Many papers on SDR require the sampling clock to have no more than 1ps of jitter [7]. Unfortunately, such low jitter clocks are not readily accessible and, in some cases, do not exist. This fact led to a deeper investigation of sampling theory and its implications for the project. After a

careful review of the theory and availability of commercially produced components, new design parameters were established with loosened jitter requirements.

The next step involved acquiring components. Obtaining what appears to be available on a company's web site turned out to be a challenge in and of itself. Through perseverance, the parts were acquired and the board layout process could begin. At this point, learning how radio frequency (RF) circuit design principles apply to this project was necessary. Due to time constraints, compromises had to be made between an optimum solution and a practical one.

1.3 Project Specifications

The goal of this development effort is to produce a reconfigurable base station capable of receiving a 1.89 GHz, Gaussian Frequency Shift Keying (GFSK) modulated, 2.5Mbps signal. At the time of this writing, the design is in the process of being debugged. The base station must produce a bit error rate (BER) no worse than 10^{-3} with a received signal of strength of –80 dBm[1] or less. The ADC's automatic gain control (AGC) must be able to properly amplify a signal ranging in strength from –80 dBm to –10 dBm, to the ADC's full dynamic range. There are no size or power constraints on the system's design. The project's guiding strategy involves placing the ADC as close to the antenna as possible, given the limitations imposed by currently-available hardware and time constraints, in order to produce a working base station with maximum reconfigurability.

1.4 Thesis Overview

Chapter 2 presents a discussion of traditional receiver architectures and the design principles for SDR. Chapter 3 presents the mixing process and the concept of phase noise, jitter, and nonlinearity. Chapter 4 examines the design constraints of receivers. Included is discussion of frequency planning, receiver sensitivity, and dynamic range. Chapters 5 through 8 outline the theory and design of the base station including: RF front end, downconversion, sampling, and digitizing the signal. Chapter 9 presents simulated results. Chapter 10 summarizes the project and suggests areas for future development. The base station's block diagram, schematic, board layout and bill of materials can be found in the appendices. The index and bibliography follow the last appendix.

[1] The Prefix Section: List of Terms and Abbreviations explains the concept of dBm.

2 Radio Receiver Background

A receiver's purpose is to take in an RF signal and output a data stream as similar to the transmitted signal as possible. Base stations gather energy from one medium, airwaves, and convert the energy into a form understandable by a user, data streams. This task involves seven steps: transducing, signal selection, unwanted signal rejection, large amplification, demodulation, error detection/correction, and, finally, received information conditioning.

These stages can be completed using a number of different architectures[2]. Regardless of the particular architecture, every base station design can be segmented into two pieces: the RF front end and the digital processor. The function of the RF front end is to receive, filter, and, if necessary, down convert the signal. The function of the digital processor is to take the digitized data stream and extract the desired information.

This division is determined by the placement of the ADC. The location and function of this division provides two matrices with which to classify base station architectures. Examining the ADC's bandwidth capabilities and location in the signal path shows the category into which a particular architecture fits. Bandwidth capabilities classify the base stations into narrow or wide band receivers. This classification is discussed in Section 2.1. The proximity of the ADC to the antenna determines how to classify base stations. The classification is based on the number of intermediate frequency (IF) stages and is equal to the number of times the signal is down converted: two down converters (mixers) means two IF, one down converter means one IF, and no down converter means zero-IF. Having zero-IF base stations is the goal of software radio and is discussed in Section 2.2.

This project fixes bandwidth of the RF front end, thereby implementing a narrowband architecture, and examines various placements of the ADC. As the ADC moves closer to the antenna, sampling problems become increasingly important. Therefore, a careful understanding of oversampling and undersampling is required to determine implications of the various ADC locations. Section 2.3 presents the theory and necessary equations needed to understand sampling as it relates to software radio base station implementation.

[2] In addition to the architectures presented below, new architectures and new chips that allow for the implementation of these architectures are hot areas of research.

2.1 Narrowband vs. Wide Band Architectures

Narrowband receivers (also called single-carrier receivers), shown in Figure 4, refer to traditional radio, where signal selection is performed using analog components. The RF front end must eliminate unwanted signals through filters that allow only the signal of interest to be presented to the ADC. Many base stations currently in use are narrowband receivers.

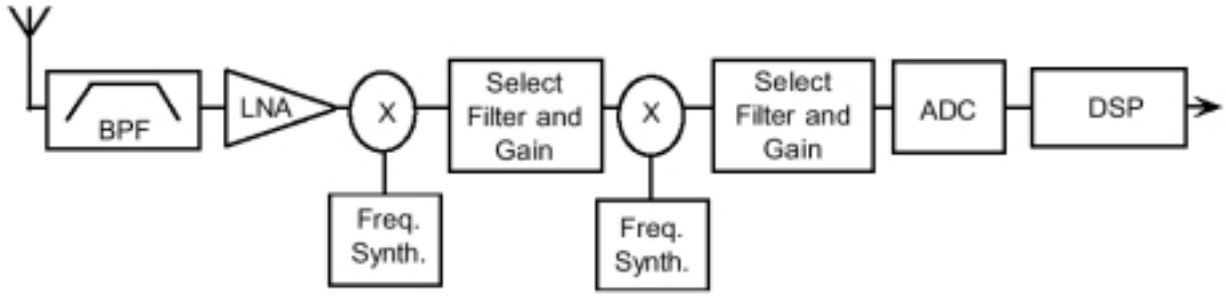


Figure 4. Typical single-carrier receiver [9]

In wideband receivers (also called multi-carrier receivers), shown in Figure 5, signal selection is performed with digital filters. Therefore, the RF front end accepts an entire band and presents it to the ADC. This method requires a wide band ADC that can simultaneously digitize multiple channels. After the ADC, filtering, tuning and processing are performed digitally. The decision to use either a narrowband or a wide band receiver results in certain implementation requirements. Single carrier receivers require a separate RF front end for each channel in a band, as illustrated in Figure 6.

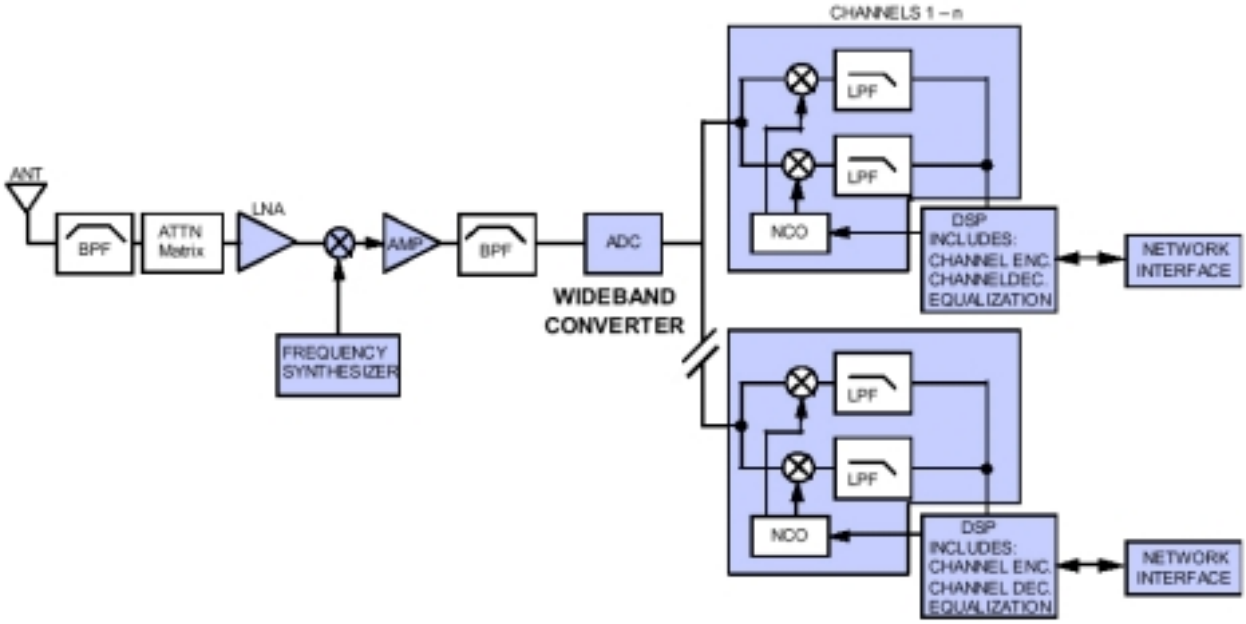


Figure 5. Typical multi-carrier receiver [9]

Generally the RF front end is unable to receive multiple channels, but in multi-carrier receivers, the RF front end is wideband and can be shared among all the channels. Thus, it is much more costly to build a base station that can receive an entire band, comprised of multiple channels, if a single-channel architecture is chosen. Prior to the development of the wide band ADC, a system designer did not have the choice between these two architectures.

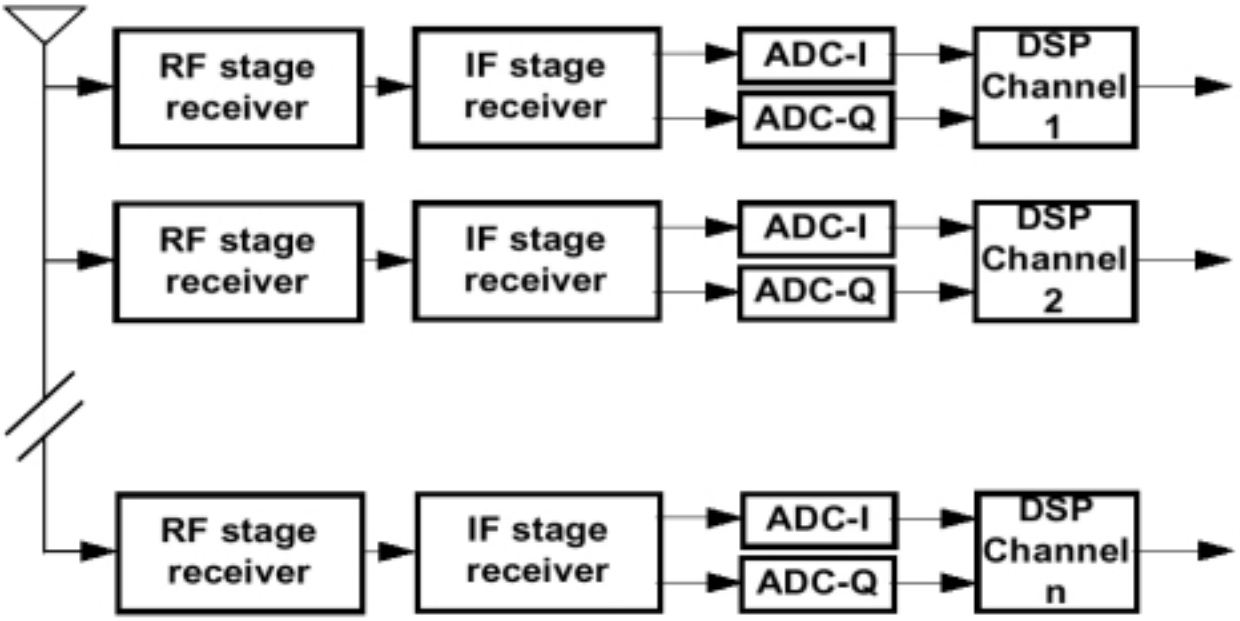


Figure 6. Narrowband architecture used in a base station receiving multiple channels [10]

Each architecture presents different requirements on the ADC. Narrowband architectures are most effected by the ADC's: signal-noise-distortion to noise-distortion ratio (SINAD), spurious-free dynamic range (SFDR), and signal-to-noise ratio (SNR). SINAD refers to the overall noise floor. SFDR indicates the degree to which strong signals interfere with signals from other channels. The SNR defines the signal strength, given a certain amount of noise. A narrowband ADC can achieve better dynamic range by using automatic gain control (AGC) to account for the range of received signal strengths and, therefore, achieve better dynamic range.

Wide band ADCs lack this advantage, since they must digitize all channels simultaneously, thereby eliminating the possibility of per channel AGC. For example, global system for mobile communications (GSM [11]) systems are required to process signals with a noise floor of –114 dBm, whose strength is between -13dBm and –104 dBm [10]. The SFDR for the ADC must be approximately 100 dBFS, to account for the required 91 dB dynamic range. In addition, GSM systems have 124 channels, each with a bandwidth of 200 kHz, requiring the ADC to have a sampling rate of at least 50 MSPS.

Meeting these tough constraints causes the base station, and especially the digital processing section, to be designed specifically for a particular standard. Since the standards continually evolve and change, the base stations must either be rebuilt each time a new standard emerges, or they have to be reconfigurable. Software defined radios are an effort to meet this need for reconfigurablity.

2.2 RF Sampling vs. IF Sampling

The goal of SDR is to convert to a digital format as close to the antenna as possible. By minimizing this distance, the number of analog components are minimized, maximizing the reconfigurability of the base station. Performance capabilities of commercially available ADCs and digital signal processing chips limit how far up the signal path the digitizing can take place.

The ultimate goal of SDR is to digitize the signal just after the antenna. Figure 7 illustrates the lack of downconversion in this scenario. When a circuit has no downconversion, it is referred to as a zero-IF, direct-conversion, or software radio base station. The advantage of this scenario is that the entire base station is reconfigurable.

The next best option would be to digitize after the filtering and amplifying of the signal, which is likely to become the standard once ADC and DSP/FPGA/ASICs have increased performance capabilities. Despite the current infeasibility of these scenarios, software radios are an active topic of research and development world-wide. For example, forums such as Software Defined Radio Forum [12] actively discuss the ramifications of this type of architecture and many ADC and DSP/FPGA manufacturers are working toward the production of the hardware to support such architectures. Figure 7 illustrates the hardware requirements for these architectures [5]:

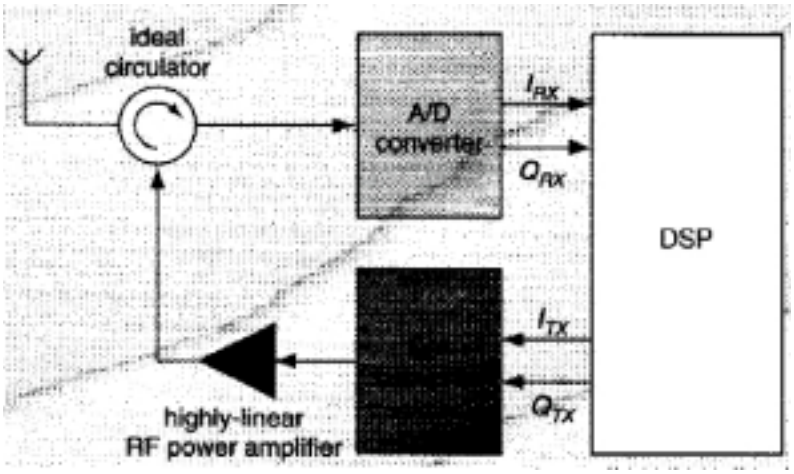


Figure 7. "Ideal" SDR with transmitting and receiving capabilities [5].

- wideband antenna with gain/loss figures around 0 dBi.
- circulator or duplexer with high isolation and broadband coverage (if the software radio needs to receive and transmit.)
- high speed (4 time the bandpass oversampling), wideband (bandwidth greater than 2.2GHz) ADC with a resolution greater than 20 bits.
- fast digital signal processing chips capable of processing the incoming data.

Although some very expensive, application-specific high-end applications do use direct-digitizing software radio [13], today's technology is generally unable to economically meet the above requirements. The best option is to downconvert a GHz signal to below 250MHz and then digitize, as shown in Figure 8. These systems employ only one mixer and perform most of the signal processing in the digital domain. Base stations with more than one IF , as shown in Figure 9, perform the filtering and downconverting in multiple stages. Therefore, base stations with two or more IF stages are usually referred to as "classical base stations" and base stations with one IF are usually referred to as IF-sampling base stations. This project explores the limitations of IF-sampling and presents a design for an IF-sampling receiver.

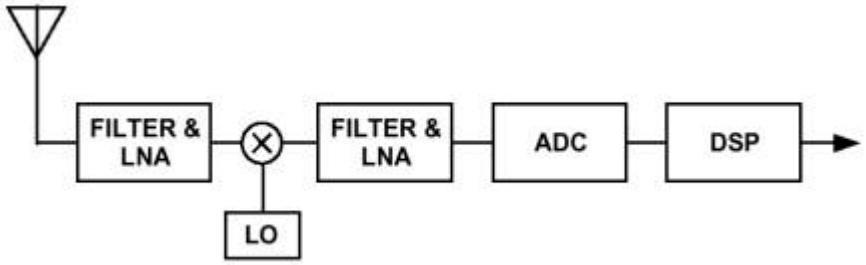


Figure 8. Digital receiver block diagram [14].

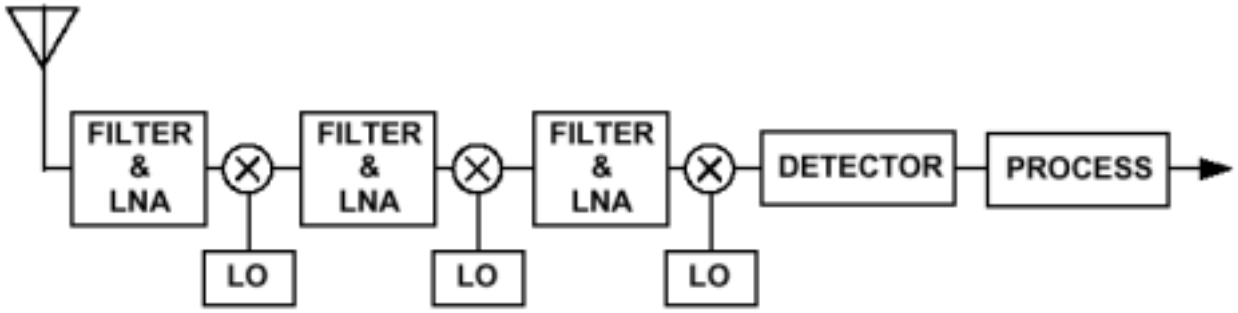
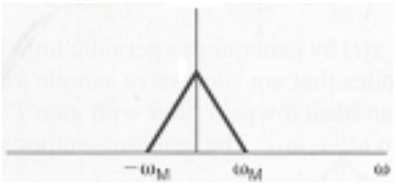


Figure 9. Typical receiver Block diagram [14].

2.3 Oversampling BW and Undersampling the Carrier

The closer the ADC is to the antenna, the more undersampled the RF or IF signal is. When a signal is undersampled (sampled below its Nyquist frequency [15, pg 529]) how can the signal be reconstructed? There are two frequency measurements of importance. The first is the carrier frequency, f_c. The second is the bandwidth of the channel, BW. Both the f_c and the BW need to be compared to the sampling frequency, f_s. In most base station applications f_c is in units of GHz, BW is in units of MHz, and f_s is in units of MHz. This is a vital fact to remember when dealing with software radios. Before a

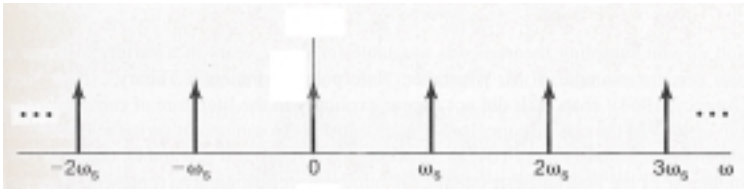
discussion of oversampling and undersampling is done, a brief review of sampling and Nyquist zones are presented.



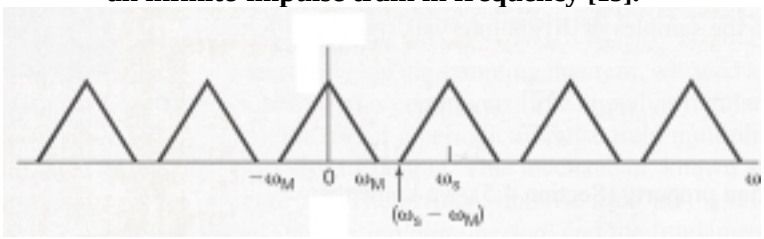
Graph 1. Frequency representation of a band limited signal that will be sampled in the time domain [15]

2.3.1 Review of Sampling

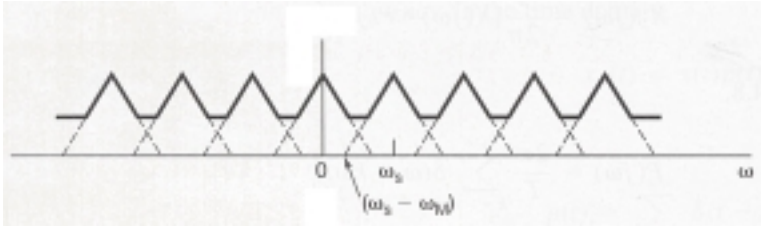
Graph 1 through Graph 4 are presented to illustrate the ideas in sampling that are important for software radio design. Graph 1 is a frequency representation of an arbitrary signal, X(jω), bandlimited between $-w_m$ and $+w_m$, that will be sampled in the time domain. Periodically sampling w_m at fixed intervals of $1/w_s$ in time, corresponds to convolving w_m with an infinite impulse train in frequency. Graph 2 illustrates this infinite impulse train. This convolution produces exact replicas of X(jω), called images, at integer multiples of w_s. When $w_s > 2*w_m$ the shifted replicas do not overlap, as shown in Graph 3. When $w_s < 2*w_m$, the images overlap and aliasing occurs, as shown in Graph 4. Therefore, to avoid aliasing, a system must impose the Nyquist rule, $w_s>2*w_m$, where $2*w_m$ is the bandwidth of the signal of interest. Oversampling occurs when $w_s >> 2*w_m$. Undersampling occurs when $w_s<< 2*w_m$.



Graph 2. Sampling in time translates to convolution with an infinite-impulse train in frequency [15].



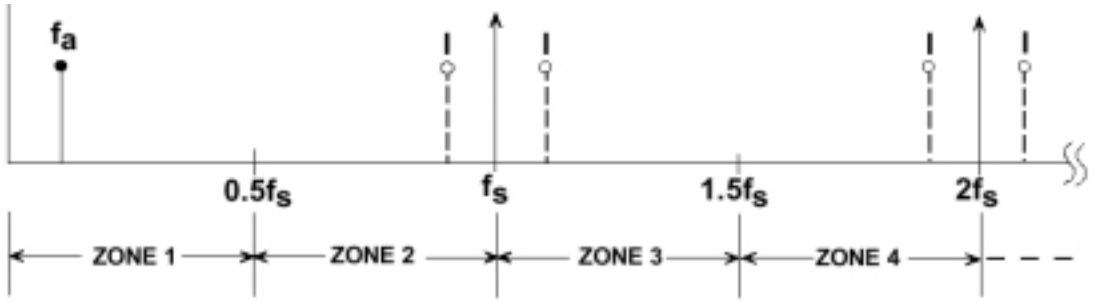
Graph 3. Frequency plot of sampled with no aliasing [15].



Graph 4. Frequency plot illustrating sampled signal with aliasing [15].

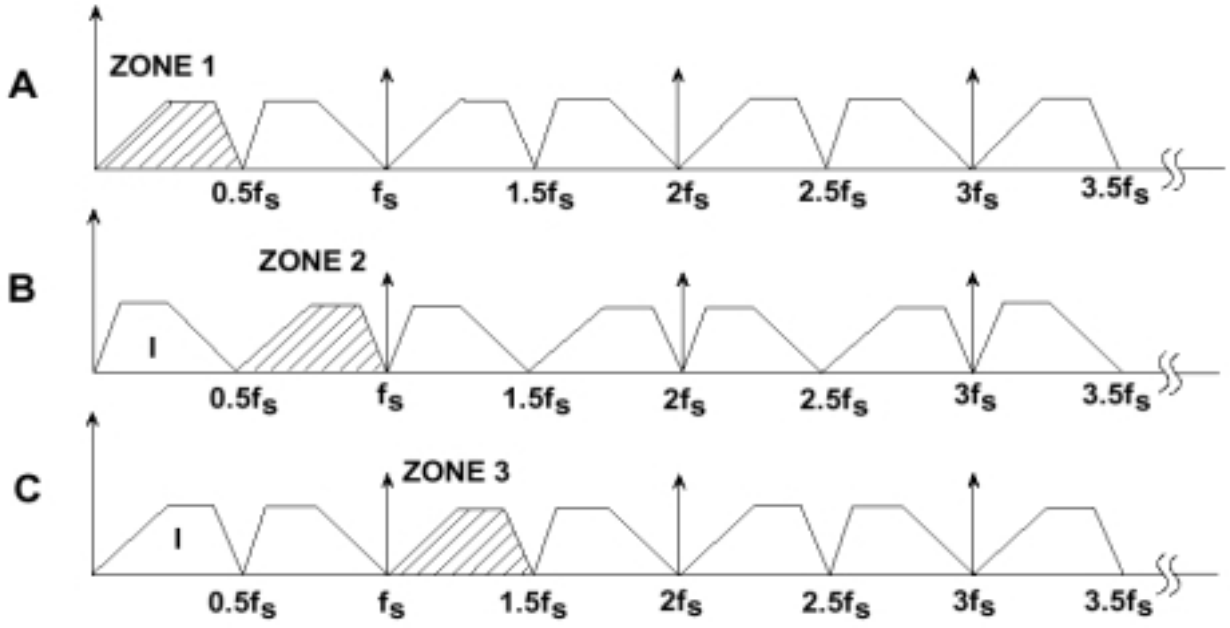
If Graph 3 is divided up into sections, at integer multiples of $w_s/2$, these sections are called Nyquist zones and their bandwidth is called a Nyquist bandwidth. Graph 5 illustrates this idea for a signal of frequency f_a, sampled at f_s. Although beginning courses on sampling theory only talk about the first Nyquist zone, DC to $f_s/2$, a careful look at the Nyquist theorem demonstrates that the other Nyquist zones are equally valid. The Nyquist criteria states:

"A signal must be sampled at a rate equal to or greater than twice its bandwidth in order to preserve all the signal information [7]."



Graph 5. Sampling f_a at f_s (see [7]).

The only constraint imposed by the above statement is that the band of sampled signals are restricted to a single Nyquist zone; sampling greater than twice the signal bandwidth will provide this. The statement does not require this zone to be the first zone. In fact the above statement says nothing about the *location* of the band of sampled signals. Provided the signals do not overlap at any multiple of $f_s/2$, theoretically any Nyquist zone can be used. The function of the anti-aliasing filter is to ensure the signals won't overlap at $f_s/2$. Graph 6 illustrates these Nyquist zones. Base band processing samples Zone 1 (Graph 6.a) and undersampling, also called harmonic sampling, uses Zones 2 or 3 (Graph 6.b[3] and c). In practice the dynamic performance of the ADC and the processor rate of the DSP/FPGA limits what Nyquist zone can be used.



Graph 6. The Nyquist zones: (a) illustrates baseband sampling, (b) and (c) illustrate IF undersampling [7].

[3] The signals are frequency flipped in Zone 2, and all even zones. This frequency reversal can be corrected by re-ordered the output of the FFT.

2.3.2 The 2nd Nyquist Zone

How do software radios use the 2nd Nyquist Zone? When a signal centered at f_c with an information bandwidth of BW is sampled at f_s, what are the constraints on f_s? Does f_s have to be twice the Nyquist frequency of f_c or of twice the BW? The answer is quite simple. When a modulated signal is sampled, there are actually two things that are being sampled, the carrier frequency and the information bandwidth [7, 16]. Therefore, f_s can be much less than the Nyquist frequency of f_c. The undersampling of f_c is acceptable as long as the BW's sampling meets the Nyquist sampling requirement, (2.1).

$$f_S > BW \tag{2.1}$$

Ensuring the sampled signal is restricted to a single Nyquist Zone is the second constraint. Satisfying (2.2) ensures the image signal is centered in the middle of the Nyquist Zone, at odd multiples of $f_s/4$, where k is a an integer. Since the carrier frequency is the frequency that is aliased down to become the image frequency, the sampling frequency can be determined by substituting $f_{carrier}$ in for f_{image} in and solving for f_s, as shown in (2.3).

$$f_{image} := (2 \cdot k + 1) \cdot \left(\frac{f_s}{4} \right) \tag{2.2}$$

$$f_s := \left(\frac{4}{2 \cdot k - 1} \right) \cdot f_{carrier} \tag{2.3}$$

The ADCs sampling clock can now be restricted to a set of frequencies, f_s, that satisfy both, (2.1) and (2.3). Oversampling occurs when $f_s >> BW$ and undersampling occurs when $f_s << f_c$. Therefore the ADC undersamples the carrier frequency, f_c, and oversamples the information bandwidth, BW. Consult [7] for an explanation on the requirements of the anti-aliasing filter to maintain a desired dynamic range when a system undersamples.

3 Mixing Phenomena

Mixing, "shifting one signal's frequency up or down by combining it with another signal" [17], is implemented twice in an IF sampling receiver. First it is used to translate a GHz (RF) signal to MHz (IF) signal, then it's used to translate the IF signal to a Nyquist zone that the ADC's dynamic capabilities can handle.

The generation of on board oscillators are required in both mixing cases. The first mixing requires the creation of a GHz signal, called the local oscillator (LO), and performs the frequency translation with the use of a device called mixer. The second case mixing requires a MHz signal, called the sampling clock, and uses an ADC to perform the frequency translation. Section 3.1 discusses the performance requirements on the LO and the sampling clock. Section 3.2 discusses the limitations of the mixing devices, and the unwanted signals that are produced from these limitations. Understanding the requirements and limitations of the frequency translation process is critical before an IF-sampling receiver can be implemented.

3.1 Oscillators

3.1.1 Mixer's Local Oscillator

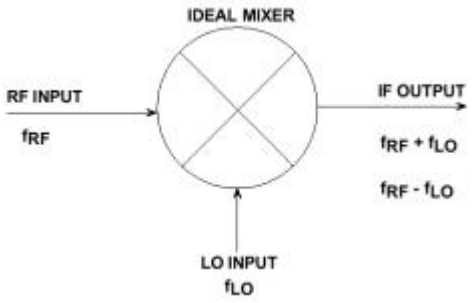


Figure 10. An Ideal Mixer [18, pg. 3-34].

The RF signal is translated to an IF signal by a device called a mixer. As illustrated in Figure 10, every mixer has three ports, the radio frequency (RF) port, the local oscillator (LO) port, and the intermediate frequency (IF) port. The RF and LO ports are inputs, whereas the IF port is an output. In an idealized mixer, the output is only a linear combination of the inputs. Phase noise on the LO causes the mixer to deviate from its ideal characteristics. [19] presents thorough description of phase noise.

Reciprocal mixing describes the phenomenon where the mixer integrates an adjacent channel's energy into the signal bandwidth. The main cause for this integration is phase noise (PN) on the LO. Just as jitter on the ADC's sampling clock effects the ADC's performance, as discussed in Chapter 0**,** the LO phase noise directly effects the mixer's performance. Although jitter and phase noise are similar,

they have different effects on receiver performance. Jitter is a wideband problem with uniform density around the sampling clock. Phase noise has a non-uniform distribution centered around the local oscillator. Phase noise decreases as the distance from the LO frequency increases. The question is: what is the maximum amount of phase noise allowable on the LO that still lets the mixer meet its requirements.

Mathematically modeling the mixing process allows the effect of LO phase noise to be quantified. In the time domain, the mixer multiplies the LO's signal with the RF's signal. Since multiplication in time translates to convolution in frequency, mixing causes the entire spectrum of the LO to be convolved with the incoming signal's spectrum. Therefore, any phase noise on the LO causes energy from spectrally near channels to integrate into the desired channel, mathematically described by Equation (3.1). This equation integrates over the signal channels' bandwidth, from f_1 to f_2. X(f) is the phase noise of the LO. P(f) is the spectral density function of the RF port's input.

$$\text{In\_channel\_noise} := \int_{f_1}^{f_2} x(f) \cdot p(f)\, df \qquad \textbf{(3.1)}$$

Setting up a scenario which isolates the effects of reciprocal mixing helps determine the amount of in-channel noise caused by LO's PN. This scenario consists of applying a full-power adjacent signal to the RF port, with the signal channel empty, and a LO with phase noise to the LO port. An adjacent signal is a signal whose frequency is just outside the frequency band of interest. This frequency band of interest is called the signal channel. The signal channel remains empty to show exactly how much the LO's PN causes the adjacent signal to enter the signal channel's bandwidth after the mixer.

The output of the IF port, In_channel_noise in Equation (3.1), can be simplified and then examined after making a few assumptions. In reality, the PN is not constant but decreases with carrier offset, but for this calculation, it is safe to assume the PN is constant across all frequencies. Therefore x(f) becomes a constant, call it LO_Phase_Noise. The second assumption is that the integrated spectral density function is simply the total signal power for a typical interferer. With these assumptions, Equation (3.1) simplifies to Equation (3.2); and in log form, Equation (3.2) simplifies to Equation (3.3).

$$\text{In\_channel\_noise} := (\text{LO\_Phase\_Noise}) \cdot (\text{Integrated\_adjacent\_signal\_power}) \qquad \textbf{(3.2)}$$

$$\text{In\_Channel\_Noise}_{\text{dBm}} = \text{PN}_{\text{dBm}} + \text{Adj\_Sig\_Power}_{\text{dBm}} \quad \textbf{(3.3)}$$

Comparing the amount of in-channel noise caused by LO's PN to the amount of in-channel noise caused by thermal effect, provides a way of setting an upper bound on the PN, as shown in Equation (3.4). This restriction requires the LO's PN's effect on system noise to be less than the thermal noise's effect. If the thermal noise contribution to system noise levels at the mixer port is the same as it was at the antenna port, the thermal noise at the mixer, can be calculated from Equation (4.3).

$$\text{PN}_{\text{dBm}} < \text{Thernal\_Noise}_{\text{dBm}} - \text{Adj\_Signal\_Power}_{\text{dBm}} \quad \textbf{(3.4)}$$

If we assume that the adjacent channel interfering signal is a typical signal, such as a global system for mobile communications (GSM) signal, then the Adj_Signal_Power is –13 dBm. And if we assume the thermal noise at the mixer is the same as at the antenna port, then the Thermal_Noise is -92.4 dBm (calculated in Section 4.3.1.1). Therefore, the phase noise on the LO must be less than –79.4 dBm with an offset of 140 MHz, for this design.

3.1.2 ADC's Sampling Clock

The ADC's sampling clock jitter directly effects the receiver's bit error rate (BER). Since jitter is the critical parameter in SDR, Chapter 0 is devoted entirely to explaining the what causes jitter, how to mathematically model it, and how much is allowable given a particular BER. Jitter is only mentioned here, in this section on requirements on frequency translation, for completeness.

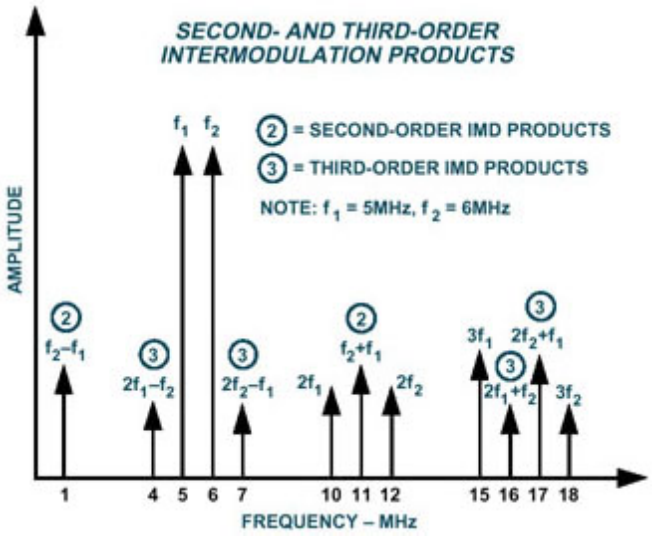
3.2 Unwanted Signals

3.2.1 Intermodulation Distortion

As the RF center frequency is set by the transmitter, the receiver must filter out unwanted signals and see only the GFSK modulated signal centered at 1.89 GHz. Section 4.1 explains why the center frequency is at 1.89 GHz. Since the receiver is a nonlinear system, signals close to the 1.89 GHz channel have the potential to distort the signal path. This phenomenon is called intermodulation distortion (IMD); the unwanted signals are called intermodulation products.

Why do intermodulation products appear? If two tones, frequencies f_1 and f_2, are applied to a linear system, the output will contain only frequencies f_1 and f_2. But, the same two tones applied to a

nonlinear system will reveal both f_1 and f_2 and signals, not at either f_1 nor f_2, but at multiples of f_1 and f_2. Examining the nonlinear system's output with a spectrum analyzer will reveal a graph similar to Graph 7. The spectral content of these "additional" signals can be understood if we model the nonlinear system's transfer function as a power series [20]. From this modeling, the spectral content of the "additional" signals are determined to be linear combinations of f_1 and f_2, thus the term intermodulation products.



Graph 7. 2nd and 3rd order ntermodulation products [21].

These IM products can produce problems if the circuit design is expecting only harmonics of the input signal to show up at the output. Figure 11 illustrates the potential problem that can arise from IMD. In this case, a signal nearby the channel of interest, while not causing a problem before the mixer, can cause quite a problem after the mixer. If the IF's location doesn't take into account potential strong signals adjacent to the signal channel, the channel information can become corrupted once it passes through the mixer.

As can be seen from Graph 7, it is easy to filter out 2nd order products since they are not near f_1 and f_2, but hard to filter out 3rd order products. The main products that need careful attention are $2f_2–f_1$ and $2f_1-f_2$. They will increase the in-channel noise if the IF is chosen such that they end up lying in the signal channel.

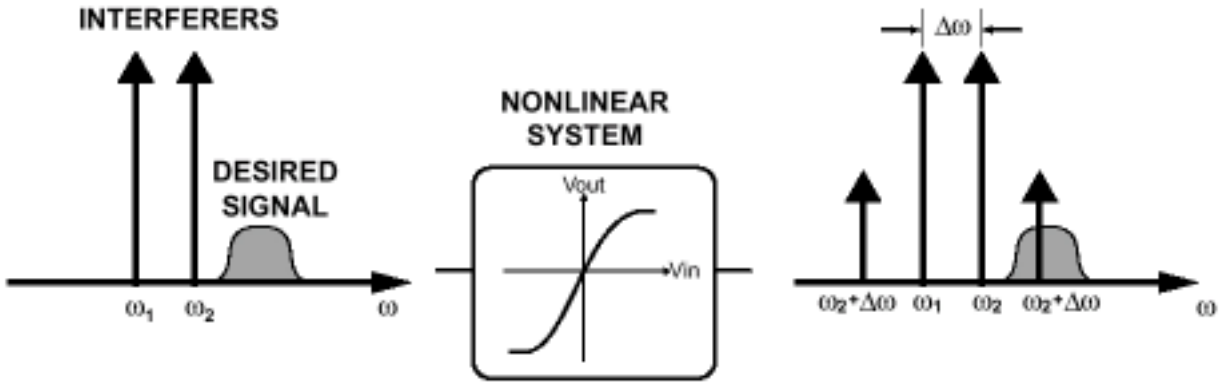
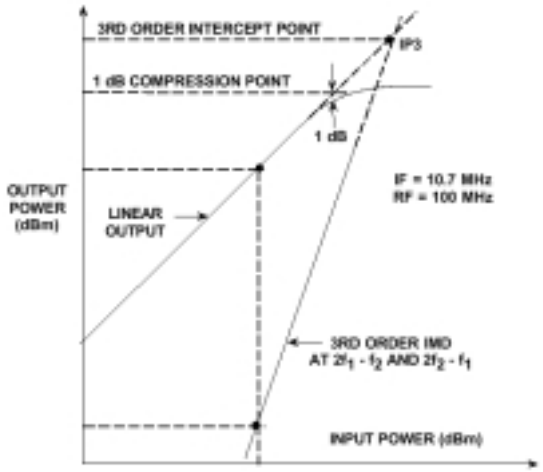


Figure 11. Illustration of nonlinear system producing undesirable intermodulation products that lie in the desired signal's passband.

Therefore, while the interfering signals are NOT initially in the channel around 1.89 GHz at the input to the receiver, they can show up in the channel and mask out small signals in the presence of larger ones. As can be seen in the graph, the 3rd order IM products, $2f_2–f_1$ and $2f_1-f_2$, lie VERY close to f_1 and f_2, and will be a problem if they end up in the center of the channel of interest. Therefore, when determining reference oscillator's frequency and the location of the IF, as discussed in Section 4.2, the location of the IM products must be considered.



Graph 8. Linearity, IMD and 1-dB compression Points [18, see 3-52].

A device's transfer function is only valid over a limited range of inputs. As the input power increases past the device's linear operating range, the output will depart from the expected transfer function. The device can no longer create the desired output given inputs outside of its operating range. The term 1-dB compression point refers to the point when a device's output level is 1 dB lower than the expected output.

The input referred third order intercept point (IIP3) and 1-dB compression points determine how strong the input signal can be before IMD products will start corrupting the signal. Therefore, the location of IIP3 and 1-dB compression points indicates the linearity[4] of the system [22]. Section 4.3.2.1 calculates the IIP3 and 1-dB compression points for this design.

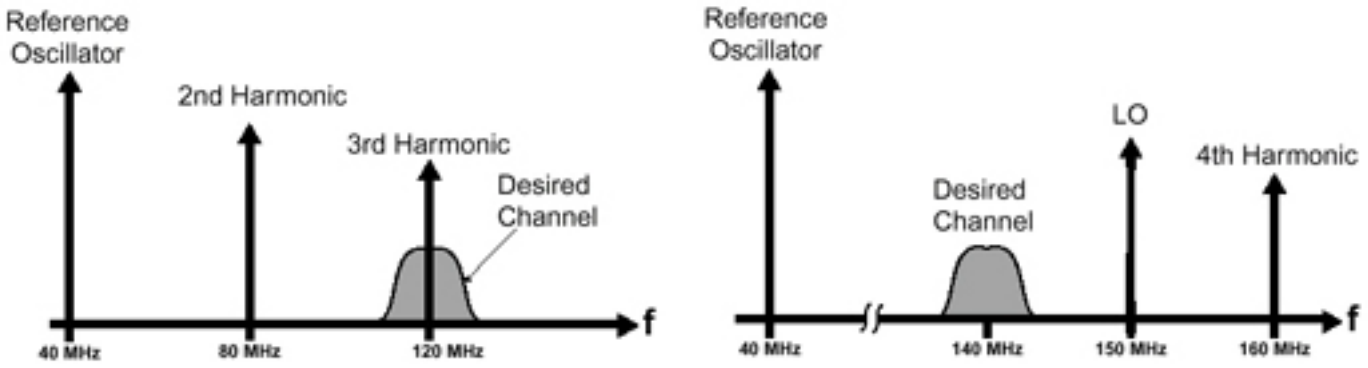
3.2.2 Problematic Harmonics

Figure 12 demonstrates how in-channel signal degradation can happen, not only by intermodulation products, but also by harmonics of on board oscillators. One such oscillator that can cause signal degradation is the "reference oscillator." The reference oscillator is the input to a phase lock loop (PLL) that produces the LO. For now, treat the PLL as a black box with one input, the reference oscillator, and one output, the LO. Section 0 will describe the PLL in detail.

Figure 12 illustrates how, given a particular reference oscillator, the location of the IF determines if in-channel signal degradation will occur. In Figure 12(a), the IF is placed at 120 MHz, therefore the reference oscillator's 3rd harmonic will fall directly into the channel of interest. In Figure 12(b), the IF is

[4] Mixers are not linear devices, but their transfer function from one frequency to another is linear. Here "linear" means that a 1-dB change in an input signal produces a 1-dB change in the output.

placed at 140 MHz, therefore the 3rd and 4th harmonic do not lie in the channel of interest. The one problem in Figure 12(b) is the proximity of the 4th harmonic to the LO. Without further, post-mixer filtering, the 4th harmonic will be translated down, with the LO, to the sampled Nyquist zone. Suppression of such unwanted harmonics are explained in Section 0.



(a) (b)

Figure 12. Location of the IF determines if a reference oscillator's harmonics cause in-channel signal degradation (a), or not (b) [23].

4 Receiver Design Constraints

4.1 Block Diagram

The overall goal of the wireless sensor project is to send sensor data wirelessly from a sensor to a computer. There are a large range of sensors that require this functionality. The data rate of these sensors ranges from high data rates (e.g. imagers) to low data rates (e.g. bend, pressure and temperature sensors). The signal path flows from a sensor to a transmitter and then through the RF airwaves; it's next received by a base station and finally processed by a computer. The European digital enhanced cordless telecommunications (DECT) frequency bandwidth, 1.88-1.90 GHz, was chosen for the design because this channel has few interferers in the Boston area and single chip transceivers are readily available [24]. This choice restricts the RF channel to be between 1.88-1.90 GHz.

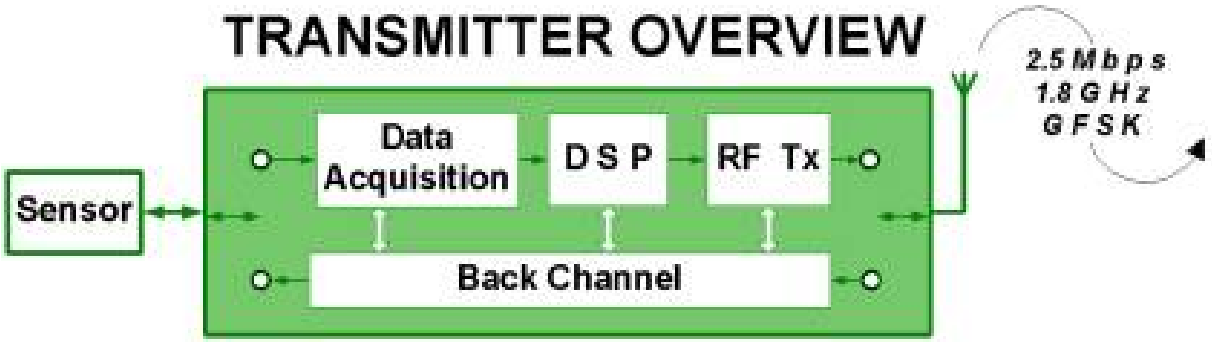


Figure 13. Transmitter block diagram.

Regardless of the type of sensor, the main function of most sensors is to produce a signal whose change in magnitude reflects the phenomena being measured. These waveforms are captured by a data acquisition system, fed to a DSP, and then modulated up to an RF frequency, as in Figure 13.

Having the ability to receive signals from a transmitter built using two custom VLSI chips from MIT's Microsystems Technology Laboratories [25] is one of the base station's design constrains. These VLSI chips are a low power frequency synthesizer [26] and a voltage controlled oscillator (VCO). The pre-built transmitter fixed the RF center frequency at 1.89 GHz and the GFSK modulation with a transmission bandwidth (BT) of 0.5. Because the BT is 0.5, the actual occupied bandwidth is 3.325 MHz [23].

The signals in the base station take in the wireless signal, downconvert, filter and then digitize, as shown in Figure 14.

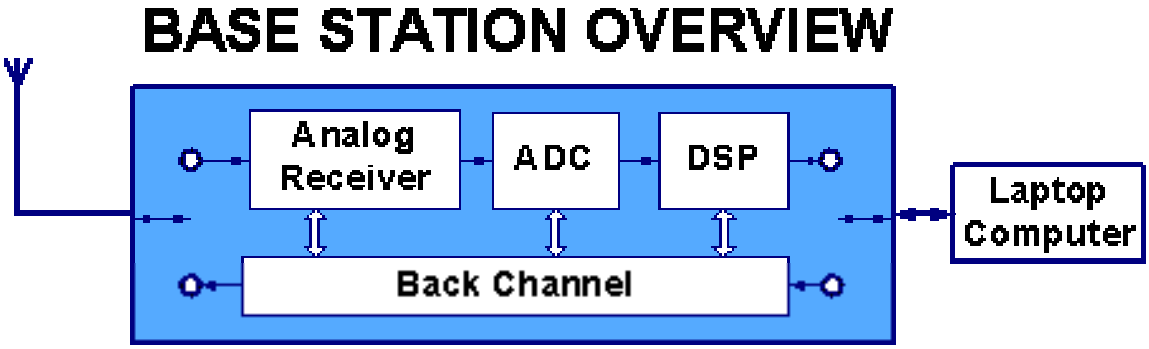


Figure 14. Base station overview.

This project accomplishes the above tasks via the stages outlined in Figure 15. These blocks are divided into an RF Board and a Digital Board.

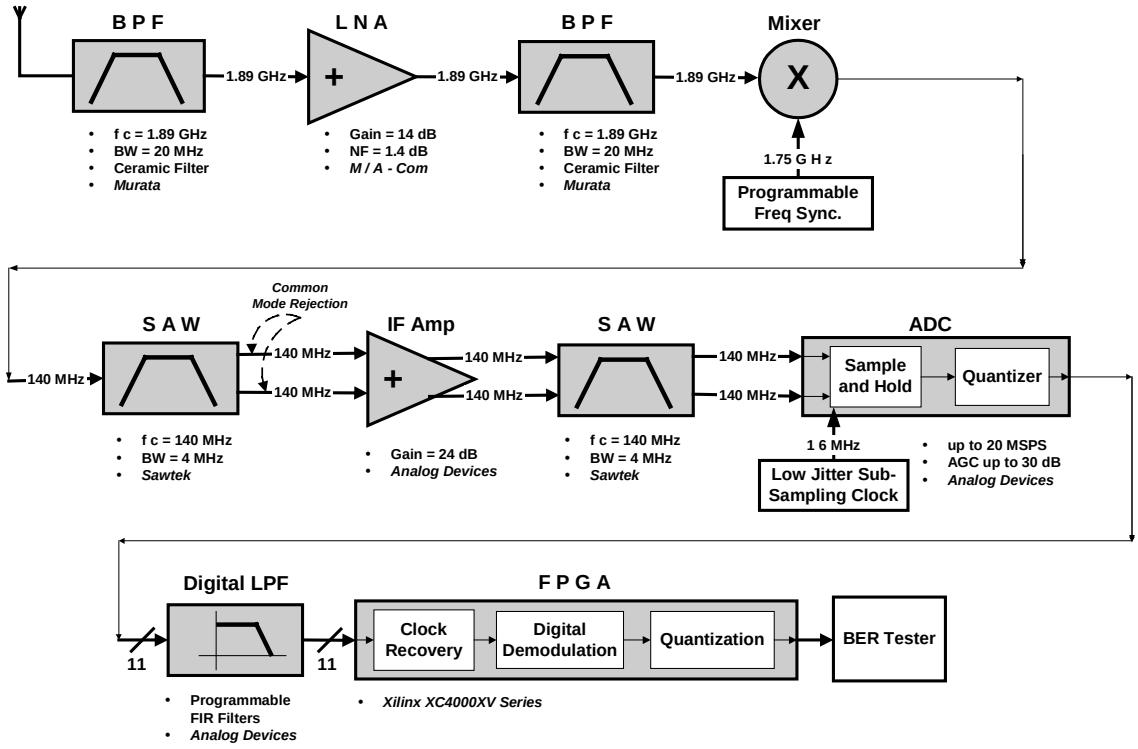


Figure 15. Detailed block diagram of base station.

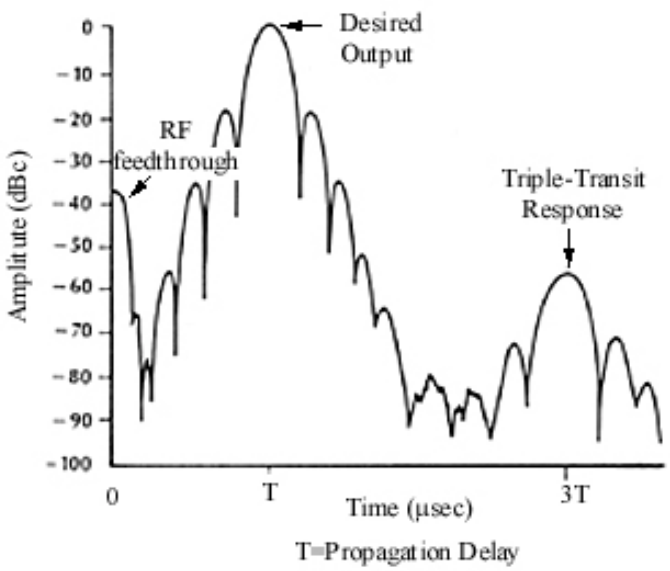
After performing a system budget analysis, constraints were placed on each block in the base station's receive path. Table 1 lists the constraints on the blocks in Figure 15.

Part	Gain	Noise Figure	IIP3
BPF	1.7 dB	1.7 dB	NA
LNA	14 dB	1.38 dB	14 dBm
BPF	-1.7 dB	1.7 dB	NA
Mixer	9 dB	8.5 dB (9mA)	0 dBm
SAW	-10.85 dB	10.85 dB	NA
IF Amp	13 dB	5 dB	5 dBm
Total Cascaded Figures	**20.90 dB**	**5.70 dB**	**-9.84 dBm**

Table 1. System Constraints.

4.2 Frequency Planning

A critical first step in the design of a wireless system is frequency planning. What RF channel can be used? Where can the IF stage be located without excessive interference? This section addresses these questions. Many commercial designs require working within the regulations of the FCC, standards committees, and other products on the market. Because this project is for research, many of the typical requirements for commercial frequency planning were neglected.



Graph 9. Impulse response of a typical SAW filter[27].

4.2.1 Choosing the IF Frequency Location

It was necessary to determine the best trade-offs between optimum IF frequency location, surface acoustic wave filter (SAW) bandwidth, and sampling clock frequency. The following parameters had to be considered: locations of potential adjacent interfering signals and IMD distortion, locations of aliased copies

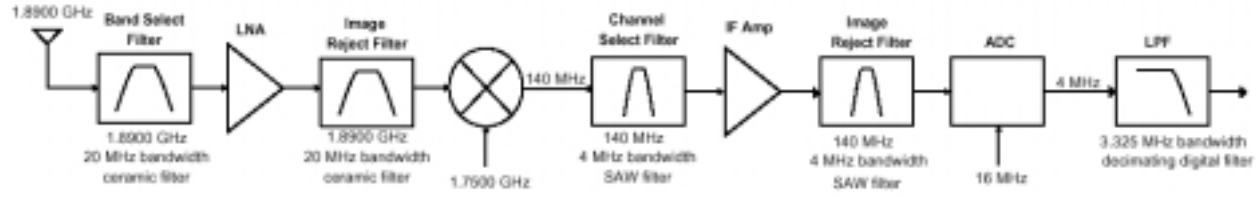
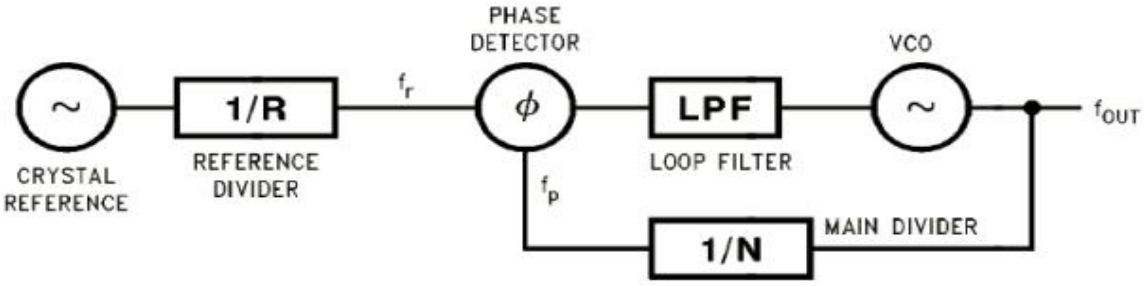


Figure 16. Frequency plans for the RF front end.

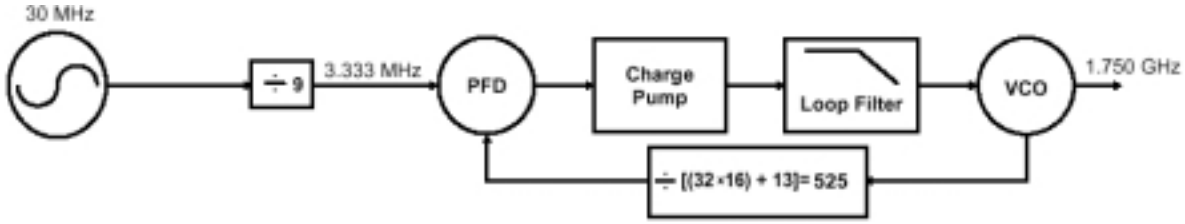
caused by the SAW filter's Triple Transit Response (see Graph 9), location of image frequencies, and availability of parts. Figure 16 illustrates the final decisions of the study: IF at 140 MHz, SAW

bandwidth of 4 MHz, and subsampling clock (f_s) at 16 MHz. These decisions caused the final signal that will be digitally processed to be placed at $f_s/4$ (4 MHz.) Having the final signal at $f_s/4$ allows the demodulation to be simplified [28]. The SAW filter's band pass properties [29] make overlap of the aliased signals occur at more than 10 dB down from their original strength. This reduces the amount of work for the digital low pass filter (LPF.)

A reprogramable frequency synthesizer was chosen to set the local oscillator frequency, in case the IF frequency had to be shifted around due to interference. Figure 17 illustrates the values chosen to program the frequency synthesizer. The reference divider has a value of 9. The main divider has a value of 525. The 30 MHz reference oscillator is divided by the reference divider and then driven into a phase detector (PD). The voltage controlled oscillator (VCO) is divided by the main divider and also driven into the PD. The PD compares the phase of the divided reference oscillator signal to the divided VCO signal. An error voltage is produced to correct for any differences in phase. This feedback loop, called a phase lock loop, produces a stable 1.750 GHz signal. This signal is the mixer's local oscillator. Section 6.2 describes the phase lock loop (PLL) theory implemented in Figure 17.



(a) Block diagram of a basic PLL.



(b) PLL values that produce this design's LO.

Figure 17. Synthesis of the mixer's local oscillator.

4.2.2 Image Rejection Filtering

Figure 18 illustrates spectrally how the location of the IF frequency effects the location of the image frequency. Figure 20 temporally illustrates the potential problem associated with image frequencies. Figure 19 displays a band pass filter (BPF) capable of suppressing the image frequency, so its effects will be less corruptive to the channel of interest.

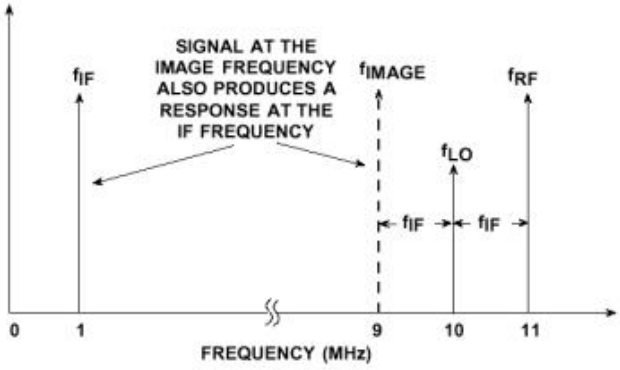


Figure 18. Image response [18, pg. 3-39].

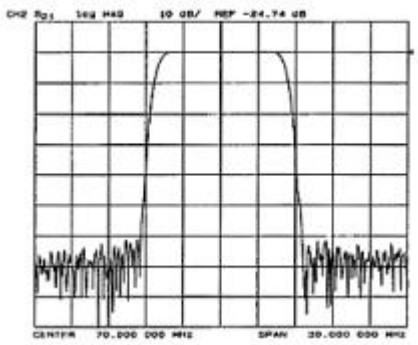


Figure 19. SAW frequency response with optimal layout [27].

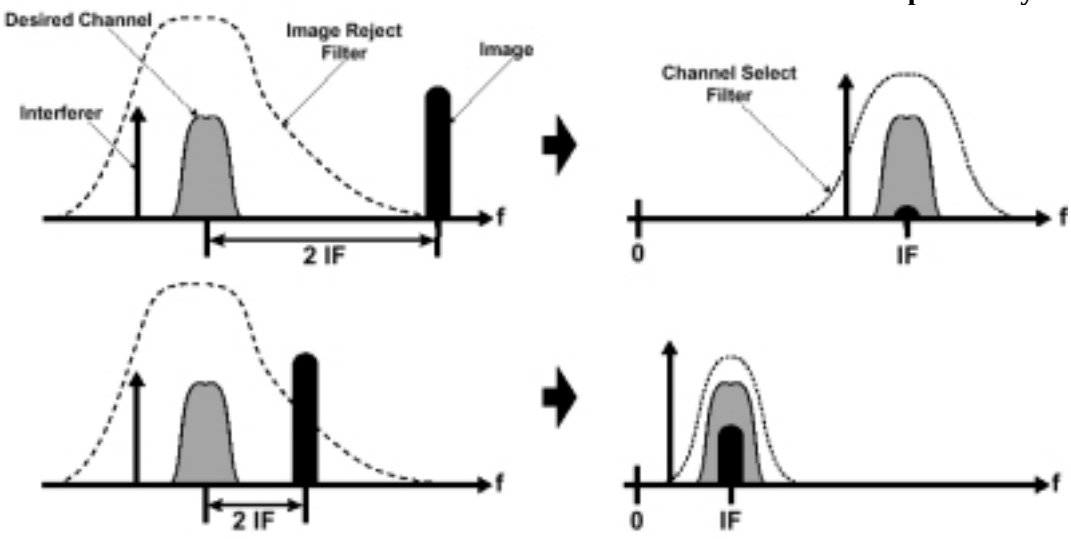


Figure 20. Importance of an image rejection filter before downconversion.

4.3 Radio Performance Limitations

This section contains a description of the signal and noise terms relevant to designing a base station. The following, often confused terms will be defined and their importance explained: noise power, noise factors, noise figures, noise floors, dynamic range, intermodulation distortion, and 3rd order intercept points. These terms allow quantification of the trade-offs and constraints in a given design and give insight into the level of performance that can be expected from the base station.

It is important to note that, while these analytical techniques will outline the receiver performance and limitations, many commercial receivers use proprietary techniques to further enhance performance, such as additional noise rejection and heterodyne elimination.

4.3.1 Sensitivity

It is necessary to determine the receiver's sensitivity in order to understand the minimum signal the receiver can pick up and still meet the SNR required by the demodulator. The demodulator receives certain SNR and demodulates the signal, meeting a given BER. In this design, the demodulator requires a SNR of 72 dB [28] requirement applies to the RF front end and the ADC. The process for finding how much the circuit reduces the available noise power is as follows:

1. Determine the noise bandwidth of the circuit.
2. Calculate the available noise power at the antenna port.
3. Calculate the noise figure of the analog section up until the ADC's input.
4. Refer this noise figure to the ADC input and convert it to a root mean squared (rms) voltage.
5. Determine and then convert all noises within the ADC, including the thermal and quantization noise, into an rms voltage.
6. Sum the analog noise figures with the ADC's input reference noise voltage.

4.3.1.1 Available Noise Power

Analog signal processing chains are, in part, characterized by the amount of noise they add to the signal. There are two noise types that can be distinguished. The first is the *existing* signal noise, which the base station will filter and amplify. This is the noise that the antenna picks up and that is present at the antenna port, called the available noise power, as seen in Figure 21. This noise is endemic to all receivers. The second is the noise the circuit adds to the signal, which is commonly termed the noise factor; it is discussed in section 3.4.2.

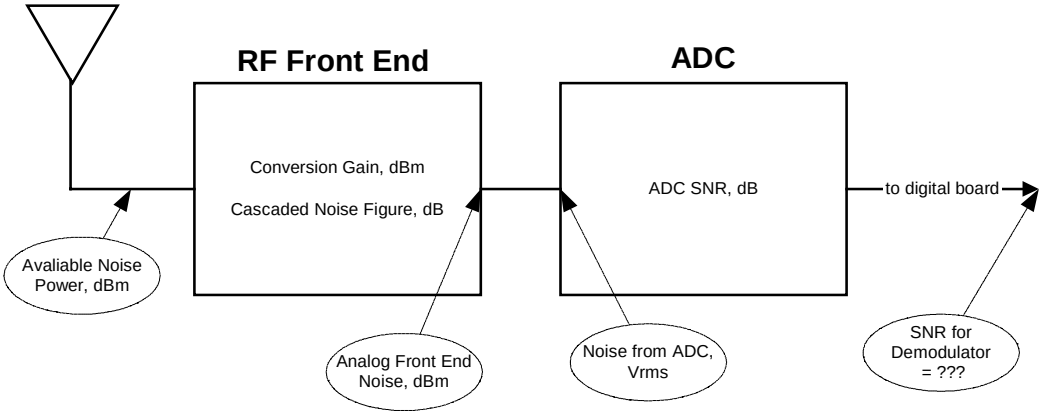


Figure 21. Sensitivity measurement calculation.

Knowing the available noise power at the antenna port provides a reference point with which the receiver's performance can be measured, and a system level budget analysis can then be calculated. We first reduce the total amount of noise power received and then reduce the amount of channel noise power. The discussion below details what effects the available noise power at the antenna port. Sections 3.4.2 and 3.4.3 explain how each stage between the antenna port and the ADC reduces the total noise power by the stage's noise figure. After the ADC, digital signal processing reduces the channel noise power, thus allowing proper recovery of the sensor signal.

Regardless of the number of iterations discovered through a Smith chart [30] and network analyzer [31-33], some impedance mismatch at the antenna port of every base station will remain. This impedance mismatch is basically a resistance. Any resistor whose temperature is greater than absolute zero exhibits noise as a result of movement in its charge carriers. This phenomenon is referred to as Johnson noise [34, 35]. The Johnson noise voltage of a resistance, R, in ohms, for a bandwidth, B, in Hz, at a temperature, T, in Kelvins, can calculated with Equation (4.1), where k is Boltzmann's constant 1.38e-23 J/K. Although all resistances in a circuit exhibit Johnson noise, only the noise voltage of an input resistor or a resistor in a high-gain front-end feedback loop will have an appreciable effect on the total circuit noise. This fact explains why the antenna port is important to understand. Equation (4.2) allows the translation of this noise voltage into the source, quantifying the available noise power at the antenna port.

$$V_n := \sqrt{4 \cdot k \cdot T \cdot R \cdot B} \tag{4.1}$$

$$P_n := \frac{V_n^{\,2}}{4 \cdot R} \tag{4.2}$$

Inserting the equation for the voltage noise caused by the antenna port's impedance mismatch, Equation (4.1), into Equation (4.2), we can now calculate the available noise power at the antenna port, using Equation (4.3). It is important to notice that the available noise power is NOT a function of impedance but is a function of bandwidth and temperature. Decreasing the bandwidth or temperature of the antenna will linearly reduce the amount of noise power entering the base station. Often, the noise figure of a stage is referred to as exhibiting "x dB above kT" noise. Equation (4.3) is the source of this expression.

$$\begin{aligned} P_n &:= k \cdot Temp_{kelvin} \cdot BW && \text{In Watts} \\ P_{dBm} &:= 10 \cdot \log\left(\frac{k \cdot Temp_{kelvin} \cdot BW}{1\ mW}\right) && \text{In dBm} \end{aligned} \tag{4.3}$$

If the antenna received nothing but the bandwidth of the channel of interest, the available noise power would be 1.368e-14 Watts. This is an oversimplification but will do for our purposes. For an explanation of how 2.5 Mbps gets translated into 3.325 MHz, given a BT of 0.5, see Section 3.2. In reality, the antenna receives quite a bit more bandwidth than 3.325 MHz. Please see Section 4.1 for a calculation of the available noise power, given the particular antennae chosen in this design.

4.3.1.2 Calculating the Noise Bandwidth

Base station's antennae usually receive a huge signal bandwidth in comparison to the actual bandwidth required to transmit the information. For this design, modulated data only takes up a bandwidth of 3.25 MHz, yet the antenna's frequency range is 1850-1990 MHz (a bandwidth of 140 MHz.) As the signal travels down the receiver's chain, it goes through a series of filters which reduce its bandwidth from 140 MHz, the antenna's bandwidth, to 3.325 MHz, the information bandwidth. The part of the circuit that most limits the signal bandwidth determines the noise bandwidth of the circuit. In base stations, the type of demodulator used determines if the RF/IF filters or the demodulator most limits the signal bandwidth. Table 2 lists some demodulators according to coherence and noncoherence.

Noncoherent Demodulators	Coherent Demodulators
Envelope Detectors	Phase Lock Loops
Foster-Seeley Discriminators	Squaring Loops
Ratio Detectors	Feedback-FM Demodulators
Pulse-Count Discriminators	Costas Loops
Quadrature Detectors	I-Q Loops
Dual-Filter Demodulators	Decision-Directed Loops
Squaring Demodulators	Lock-In Amplifiers[5]

Table 2. A list of noncoherent and coherent demodulators[22].

Some demodulators, called coherent or synchronous demodulators, employ the use of a PLL to avoid a drop in receive signal power caused by phase incoherence between the transmitter and the receiver [36, page 387]. Since these demodulators most limit the received signal's bandwidth, the bandwidth of the demodulator determines the receiver's noise bandwidth. The closed loop 3 dB bandwidth for coherent demodulating receivers, B_L, determine the noise bandwidth, B_N, as in Equation (4.4). Satellite system receivers are an example of receivers which employ coherent demodulators. In this example, the coherent demodulator is capable of tracking a signal over a large frequency range, much larger than the information bandwidth, to accommodate for large amounts of Doppler shift [22].

$$B_N := 3.2\, B_L \qquad \textbf{(4.4)}$$

Demodulators that do not check for phase coherence are called non-coherent demodulators, or balanced discriminators. The RF/IF filters have a bandwidth smaller than the demodulator's bandwidth.

[5] Lock-in amplifiers use the process of synchronous detection to recover signals that have been buried in noise. They act as extremely narrow pass band filters with the pass band center point selected by a reference signal.

The 3 dB bandwidth of the most limiting filter determines, B_{3dB}, the noise bandwidth for noncoherent demodulating receivers, B_N, Equation (4.5). In tuned-radio frequency (TRF) receivers, the RF filter determines the noise bandwidth, while in super-heterodyne receivers, the IF filter determines the noise bandwidth.

$$B_N := B_{3dB} \tag{4.5}$$

4.3.1.3 Noise Factors and Noise Figures

Each block in the receiver chain has a noise figure associated with it. This section describes the concept of noise figures and the relevant equations, gives some examples, and mentions how to measure the noise figure in some particularly interesting cases. The next section explains how to calculate the cascaded noise figure, a number used to determine how the receiver chain, as a whole, reduces the available noise power at the antenna port.

First, a definition of the terms noise factor and noise figures is presented. The noise factor and noise figure terms relate to noise power issues. The distinction between factor and figure is simply a difference of units. Noise factor, F, is a numerical ratio, shown in Equation (4.6); the noise figure, NF, is simply the noise factor converted to decibels, as in Equation (4.7). Note that noise factors are expressed in non-log form while noise figures are expressed in logarithmic, dBm, form.

$$\text{Noise\_Factor} := \frac{\text{Noise\_at\_output\_port}}{\text{Noise\_at\_output\_port\_due\_to\_source\_resistance\_alone}} \tag{4.6}$$

$$\text{Noise\_Figure} := 10 \cdot \log(\text{Noise\_Factor}) \tag{4.7}$$

The noise factor is a quantity that compares the noise performance of a device to that of an ideal (noiseless) device. Here, noise performance is expressed in terms of noise power output, as in Equation (4.8), and is measured with a resistive source, as shown in Figure 22. Since an ideal device's noise power output is due to the thermal noise power of the source resistance[6], Equation (4.8) can be rewritten as Equation (4.9)[7]. Similarly, the noise factor can also be calculated as the ratio of input and output SNR, Equation (4.10).

---

[6] The voltage must be measured across a resistor in order to convert from a noise voltage measurement to a power measurement, $P := \frac{V_{rms}^2}{R}$.

[7] The standard temperature for measuring the termination resistor's thermal noise is 290K.

Figure 22. Resistive source used for noise factor measurements[34].

$$\text{Noise\_Factor} := \frac{\text{Noise\_power\_output\_of\_actual\_device}}{\text{Noise\_power\_output\_of\_ideal\_device}} \tag{4.8}$$

$$\text{Noise\_Factor} := \frac{\left(V_{no}\right)^2}{4 \cdot k \cdot T \cdot B \cdot R_s \cdot A^2} \tag{4.9}$$

$$\text{Noise\_Factor} := \frac{SNR_{out}}{SNR_{in}} \tag{4.10}$$

There are three points to consider when calculating noise factors. First, for passive devices, the noise figure is equal to the insertion loss, IL, in Equation (4.11). Insertion loss is a term used to describe the signal degradation through the device. Therefore, the IL is equivalent to negative gain, as in Equation (4.12). Second, the total noise figure for passive components in series is the summation of the individual noise figures for each component. The total noise figure for cascaded active devices is a bit more complicated and is discussed in section 4.3.1.4. Finally, if a mixer's specification sheet doesn't list a noise figure, the insertion loss for that mixer can be used [9].

$$\text{Noise\_Figure} := \text{Insertion\_Loss} \tag{4.11}$$

$$\text{Insertion\_Loss} := -\text{Gain} \tag{4.12}$$

The following, is a discussion of how to measure noise factors in active devices. Henry Ott [34] derived the formula in Equation (4.13), using the setup depicted in Figure 23.

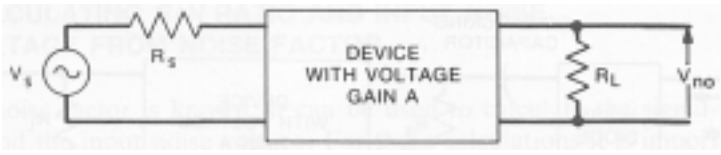


Figure 23. Set-up for measuring single-frequency (spot) noise factors [34].

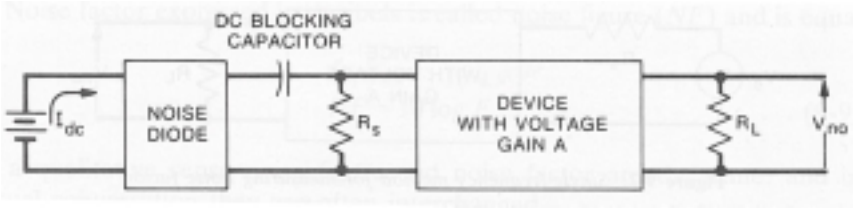


Figure 24. Noise-diode method of measuring integrated noise factors, i.e. white noise[34].

$$\text{Noise\_Factor} := \frac{V_s^{\,2}}{1.6 \cdot 10^{-20} \cdot V \cdot R_s} \qquad \textbf{(4.13)}$$

This formula demonstrates some useful points about noise factor measurements:

1. Noise factors are independent of load resistances.
2. Noise factors depend on the source resistance.
3. Noiseless devices have a noise factor equal to one.

Noise factors have three primary limitations. First, a direct comparison of two devices' noise factors is only meaningful if their noise factors have been measured with the same source resistance, bias conditions, frequency, and temperature. Second, knowing the noise factor for a device with a particular source resistance reveals nothing about what that same device's noise factor would be, given a different source resistance.

Finally, the bandwidth term in Equation (4.9) yields two methods for specifying the noise factor: integrated noise and spot noise. The first, integrated or averaged noise, requires measuring noise over a specified bandwidth. This is called the white noise method; the basic idea here is to use a forward biased diode as a white noise source, as in Figure 24. Equation (4.14) is the formula for calculating shot noise current of a forward based diode [34, page 247]. If the values of the source resistance and the noise bandwidth, are known, the integrated noise factor can then be calculated using Equation (4.15). See [34] for a derivation of this formula. Neither the bandwidth nor the gain of the device need to be known when calculating the integrated noise factor by the diode method. Unfortunately, spot noise calculations, Equation (4.12), require knowledge of the noise bandwidth of the device. Equation (4.12) assumes the source resistance is at room temperature Figure 23 illustrates the set-up needed to measure spot noise.

$$I_{shot} := \sqrt{3.2 \cdot 10^{-19} \cdot I_{dc} \cdot B} \qquad \textbf{(4.14)}$$

$$\text{Noise\_Factor} := 20 \cdot I_{dc} \cdot R_s \qquad \textbf{(4.15)}$$

The above measurement techniques work well for two-port devices but cannot work for a four-port device. In this design, the IF amplifier is a four-port differential amplifier. To varify the noise figure specification in the IF amplifier's specification sheet [38], one can either use a four-port noise figure analyzer or employ the clever technique presented in Abidi and Leete's article "De-Embedding the Noise Figure of Differential Amplifiers [37]." This paper extends Friis' two-port cascaded noise figure equation to three-ports. Friis's three-port equation is presented in section 4.3.1.4. Three-port baluns typically surround a differential amplifier, as in Figure 25. Abidi and Leete's paper present a way of calculating the noise figure for the surrounding baluns that allows for an experimental way of testing the noise figure of a differential amplifier, i.e., extrapolating a four-port noise figure measurement from a series of two-port noise figure measurements. The basic procedure for finding the noise factor, F, and the gain, A, of the "Device Under Test", the differential amplifier, in Figure 25, is as follows:

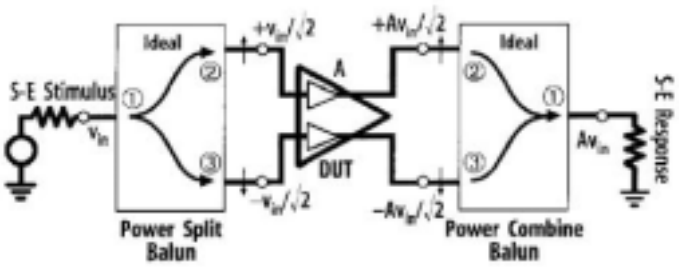


Figure 25. Differential amplifier, with gain A, surrounded by two ideal baluns [37].

1. Calculate the noise factor, F_{casc}, and gain, G_{casc}, from the left hand port one to the right hand port 1 of Figure 25.
2. Calculate the noise factor, F_1, and gain, G_1, from port 1 to port 2 of Figure 26(a).
3. Calculate the noise factor, F_2, and gain, G_2, from port 1 to port 2 of Figure 26(b).
4. Use Equation (4.16) and Equation (4.17)[8] to solve for the two unknowns, A and F.

$$F_{casc} := \left(\frac{1}{2}\right) F_1 + \left(\frac{1}{2}\right)\cdot\frac{(F-1)}{G} + \left(\frac{1}{4}\right)\cdot\frac{\left(F_2-2\right)}{\left(A\cdot G_1\right)} \qquad \textbf{(4.16)}$$

$$G_{casc} := 4\cdot G_1\cdot A\cdot G_2 \qquad \textbf{(4.17)}$$

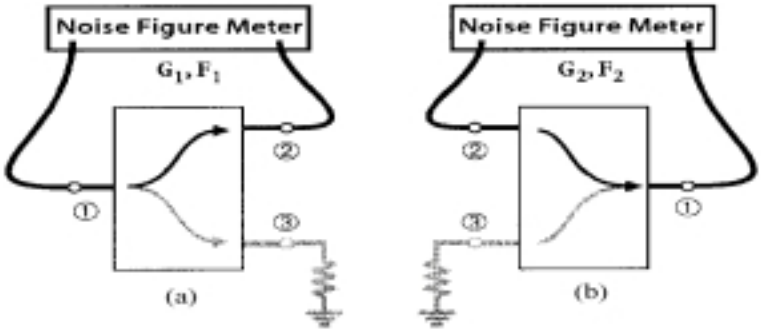


Figure 26. Test set up for a two port measurement of noise figure and gain on (a) power-splitting balun and (b) power-combining balun [37].

[8] These equations are cleverly derived Abidi and Leete's paper by carefully taking noise correlation into account.

4.3.1.4 Cascaded Noise Figures

The previous section required a calculation of the cascaded noise figure, as in Figure 27, from the analog section between the antenna and the ADC. Some of these analog devices are active, so their noise figures cannot be summed, as was done with passive devices. Friis derived an equation, Equation (4.18), for the total cascaded noise figure of active devices, referenced to the input port. Notice that the noise of the first stage adds directly to the overall noise figure, while all subsequent stage's noise figures are divided by the total gain of all stages up to that point. Therefore, the noise figure of the first active device is critical, explaining why the first active device after the antenna is a low noise amplifier. The IF amplifier can afford to have a higher noise figure since, before its noise figure is added to the overall noise figure, its noise figure will be divided by the total gain up to that point.

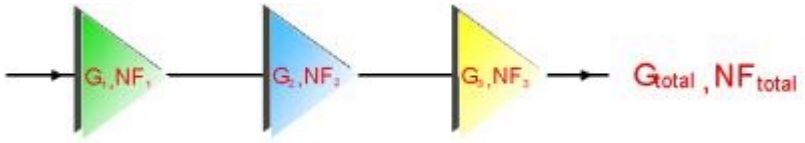


Figure 27. Block diagram of cascaded noise figure [39].

$$NF_{total} := NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 \cdot G_2} + \ldots \quad \textbf{(4.18)}$$

$$G_{total} := G_1 \cdot G_2 \cdot G_3 \cdot \ldots \quad \textbf{(4.19)}$$

When Friis's equation is applied, it references all component noise to the antenna port. Thus, the available noise, calculated in Section 4.3.1, is degraded directly by the total noise figure. Therefore, the total noise figure at the output, P_{total} in Equation (4.20), is simply the sum of the cascaded noise figure of all analog components between the antenna port and the ADC.

$$P_{total} := P_a + NF_{casc} + G \quad \textbf{(4.20)}$$

4.3.1.5 Conversion Gain

The gain of the mixer is a function of its reflection coefficient, which is a function of how well the impedances are matched at the RF and IF ports. Basically, the better matched the RF port, the more conversion gain the mixer has. For a thorough discussion of this process consult [31].

4.3.1.6 Noise Characterization for ADC

Prior to the ADC, it's easiest to work with noise figures. However, ADCs are basically voltage devices and noise figures deal with noise power issues. So, while a noise figure could be assigned to the ADC, it's often easier to work with ADCs in terms of noise voltages. Figure 21 shows how the RF front end is characterized by dBm and the ADC is characterized by V_{rms}. Finding the noise degradation within the receiver due to ADC noise sources requires these simple steps:

1. Convert the ADC's full scale V_{pp} input range to V_{rms}, using Equation (4.21).

$$V_{rms} := \frac{V_{pp}}{2 \cdot \sqrt{2}} \tag{4.21}$$

2. Find the ADC's typical SNR from the ADC's specification sheet.
3. Use Equation (4.22) to find the V_{rms} noise for the ADC.

$$V_{rms\_adc\_noise} := V_{rms\_adc} \cdot 10^{-\left(\frac{SNR_{ADC}}{20}\right)} \tag{4.22}$$

Step three is the ADC's equivalent input referred V_{rms} noise value, which includes both thermal and quantization noise.

4.3.1.7 Sensitivity Calculation

Dan McMahill [40], a PhD student at MIT's Microsystems Technology Laboratories [25],wrote a simple Cascade Analysis Program, [41], to assist in analyzing noise and distortion performances of cascaded networks. The program reads in a text file containing each element's gain, noise figure, and third order intercept point and produces a report detailing the performance at each stage. Third order intercept points are discussed in Section 4.3.2.1. Figure 28 is a block diagram representing typical values for such a text file. For this design's parameters, the output of the Cascade Analysis Program shows a cascaded noise figure of 5.7 dB and a IIP3 point of –9.84 dBm.

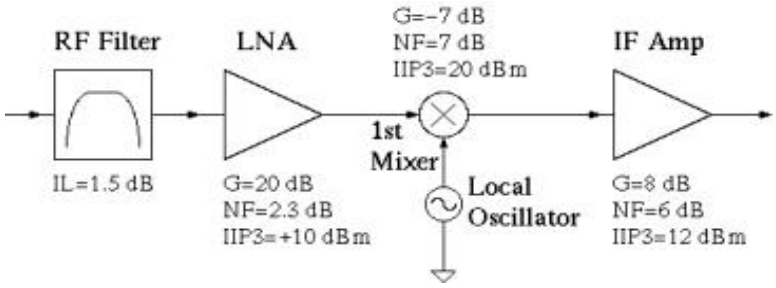


Figure 28. Block diagram with typical gain, noise figure, third intercept points information.

4.3.2 Dynamic Range

What maximum input signal range can the receiver take in and still meet all of its specifications, including gain, SNR, and suppression of distortion? This "input signal range" is the best operating region for the receiver and is called the spurious-free dynamic range (SFDR). The calculation for SFDR requires knowledge of the receiver's noise floor and third order input intercept point. Designers must choose between trade-offs of channel bandwidth and dynamic range, as shown in Figure 29.

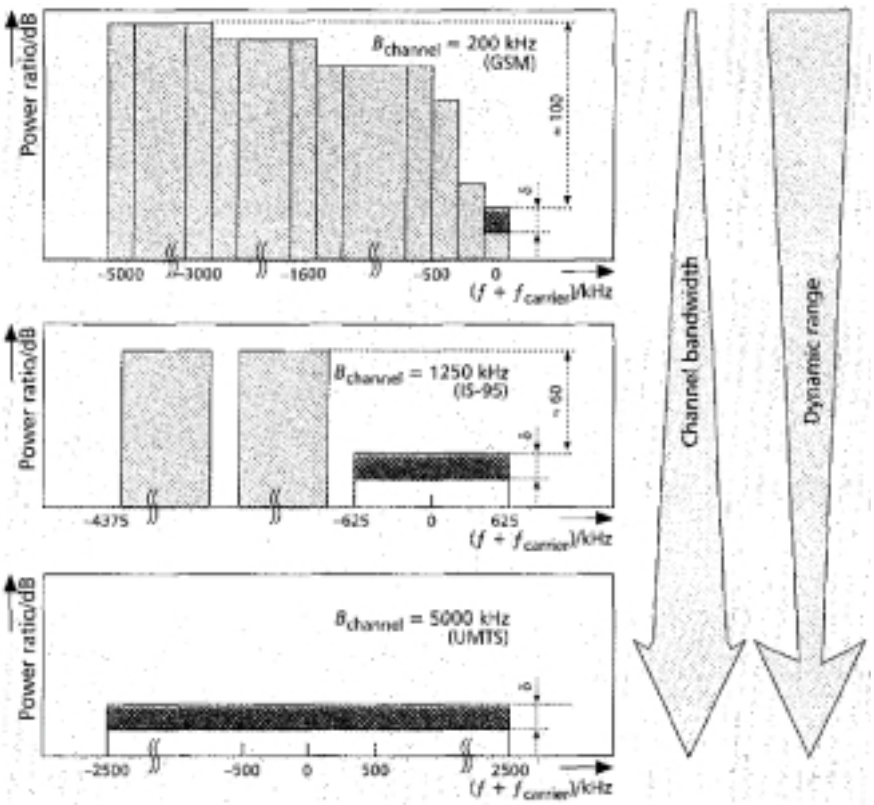


Figure 29. An illustration of bandwidth-dynamic range trade-offs [42].

Beyond a certain point, as the input signal level increases, the output doesn't continue to follow the normally expected transfer function. The output signal begins to compress. The increased level of intermodulation (IM) products cause this compression. Section 3.2.1 explains IM products. Examining the spectral components of the compressed signal will verify this fact. This compression is characterized by the 1-dB and IIP3 points.

Noise Floor

The noise floor is the lower limit of the SFDR. Equation (4.23) illustrates how the noise floor is the difference between (1) the maximum signal level the receiver can take in without compressing the output and (2) the intermodulation power. Razavi derived Equation (4.24) in RF Microelectronics [43]. The noise floor signifies the total integrated noise of the system.

$$\text{Noise\_Floor} := \text{max\_input\_signal\_level} - \text{intermod\_power} \quad \textbf{(4.23)}$$

$$\text{Noise\_Floor} := -174\frac{\text{dBm}}{\text{Hz}} + \text{Noise\_Figure} + 10\cdot\log\left(\text{BW}_{\text{noise}}\right) \quad \textbf{(4.24)}$$

4.3.2.1 1-dB Compression and IIP3 Points

The 1-dB compression point and the third order intercept point, (IIP3), define the receiver's ability to accept large signals. Both characterize when and how the receiver's transfer function becomes nonlinear, as in Figure 30. This nonlinearity causes intermodulation products to appear, as discussed in Section 3.2.1.

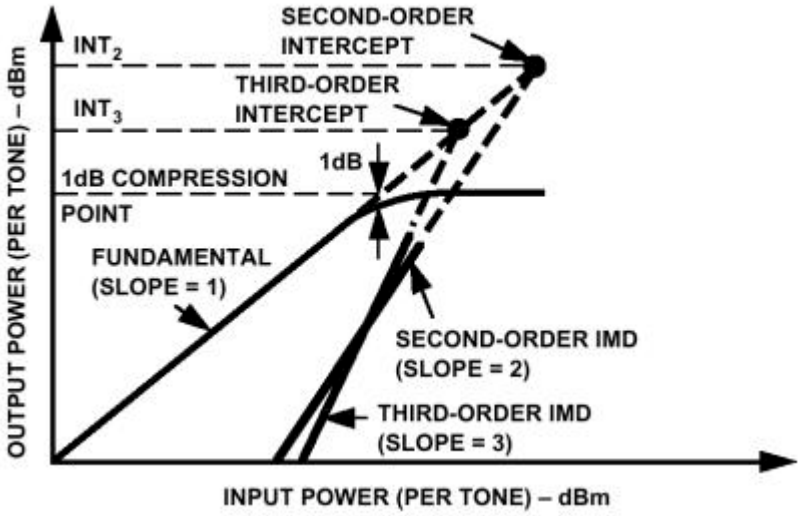


Figure 30. Intercept points, gain compression, IMD [21, pg 25]

The questions that must be answered are: to what degree is the output limited when its saturation point is reached, how does it behave in the transition region from linearity to saturation, and where is the saturation level? For low input levels, the gain remains constant. As the signal levels increase, the gain veers away from its expected value. The 1-dB compression point is the input power level that causes the output power level to drop by 1 dB. The 1-dB compression point indicates the ceiling of the receiver's dynamic range.

While the 1-dB point can be directly measured, the IIP3 point can only be extrapolated from measurements, as in Figure 30. The series of measurements leading to the calculation of the IIP3 point is called the two tone test. This test involves: (1) applying two spectrally pure low-level signals at frequencies f_1 and f_2 to a nonlinear device, (2) measuring a few IMD product terms at the output, and (3) extrapolating the 2nd and 3rd order IMD lines. This will produce a graph similar to Figure 30. The IIP3 and 1-dB compression points can be read off this graph.

Taking a few IMD measurements at the output of the two-tone test involves a few steps in order to create a graph for IIP3 and 1-dB compression:

1. Measure the output signal power, in dBm, for a single tone. The graph of this result is called the fundamental.
2. Measure the 2nd and 3rd order products and graph them.
3. Extrapolate the graphs to see where they intercept.

The end product will be two identical graphs of input vs. output power; one will be for the first tone, f_1, and the other will be for the second tone, f_2. The units of the graphs are dBm, since dBm is a power measurement unit. From the mathematics and the experimental results, it can be shown that 2nd order terms increase by 2 dB for every 1 dB of signal increase, while 3rd order terms increase by 3 dB for every 1 dB of signal increase.

Since the IIP3 point is beyond the maximum operating levels of the receiver, it only characterizes the overall linearity of the design, while the 1-dB compression point conveys the actual upper-level boundary. The 1-dB compression point is the point at which the output signal has started to be limited and is attenuated by 1 dB from the ideal input/output transfer function.

4.3.2.2 SFDR

The SFDR represents the "maximum relative level of interferers that a receiver can tolerate while producing an acceptable signal quality from a small input level" [43, pg 50]. In other words, over what range of input signal will the receiver not compress the output with no spurious signal above the receiver's noise floor. The term "compress" simply means that the transfer function is no longer linear, and the output is lower in level than expected: it is compressed. Figure 30 illustrates the concept of "compression." The concept of SFDR is shown in Equation (4.25). Once the noise floor and the third order intercept point, IIP3, are known, Equation (4.26) can be used to calculate SFDR.

$$\text{SFDR} := \text{max\_input\_signal\_level} - \text{Noise\_Floor} \quad \textbf{(4.25)}$$

$$\text{SFDR} := \frac{2}{3} \cdot \left(\text{IIP}_3 - \text{Noise\_Floor} \right) \quad \textbf{(4.26)}$$

5 RF Front End

Now that the design constraints have been established, the topology of the various stages must be determined. As shown in Figure 15, the topology includes the RF front end block, the downconversion block, the IF filtering block, the ADC block, and finally the digital block. This section explains the RF block. Chapter 0 explains the downconversion block. Chapter 0 outlines the requirements on the sampling clock. The concepts involved in digitizing a modulated signal is discussed in Chapter 0.

The RF block's function is to receive a wireless signal through the antenna, and output a signal that has more gain and is band limited.

5.1 Antenna

The Antenna is a critical and often overlooked factor in determining the range, reliability and legality of any RF-based product. Antennae are transitional structures between free-space and a transmitting source or receiving device. Antennae come in various forms depending on the application: wire antennae (Figure 31), aperture antennae (Figure 31), microstrip antennae (Figure 33), array antennae (Figure 34), reflector antennae, and lense antennae [44]. Table 3 illustrates how each form has a different amount of gain, beamwidth, and bandwidth. Wireless applications often use wire, microstrip, or array antennae. This project is designed to work with both a wire antenna, Section 5.1.1, and a microstrip antenna, Section 5.1.2. Section 5.1.3 explains how commercial base stations often are required to cover areas larger than one room, and therefore need different types of antennae.

Antenna type	Gain (dBi)	Beamwidth	Bandwidth
Omnidirectional			
Dipole	2.1	Up to 40°	Up to 60%
Stacked dipole	Up to 14	Down to 4°	Up to 23%
Discone	2.1	Up to 40°	Up to six octaves+
Directional			
Corner reflector	Up to 12	30°H/30°E	Up to 23%
Yagi array	Up to 12 (six element)	40°H (vertical polarity)	Up to 10%
Log-periodic array	Up to 12	40°H (vertical polarity)	Up to two octaves
Helix	Up to 15	40°H/40°E	Up to 10%
Parabolic	Up to 60	Down to 0.2°	Up to 10%

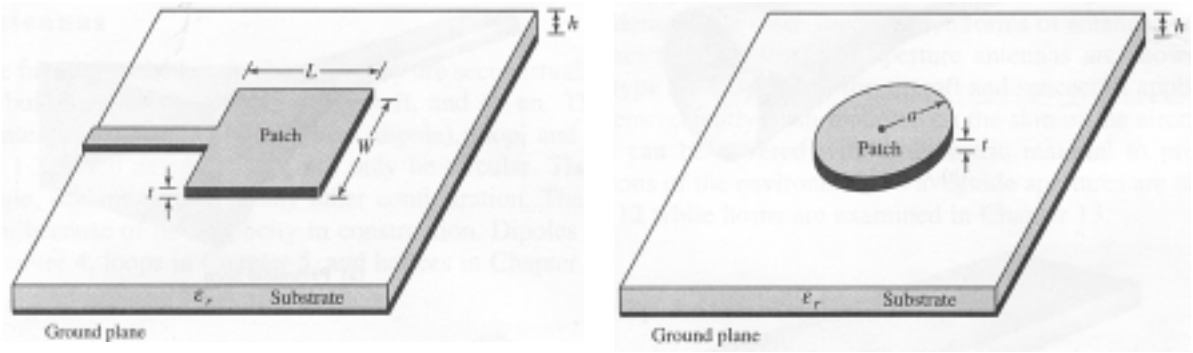
Table 3. Characteristics of Common Fixed Antennae [22, page 291].

Straight dipole Circular (square) loop Helix

Figure 31. Wire antenna configurations [44].

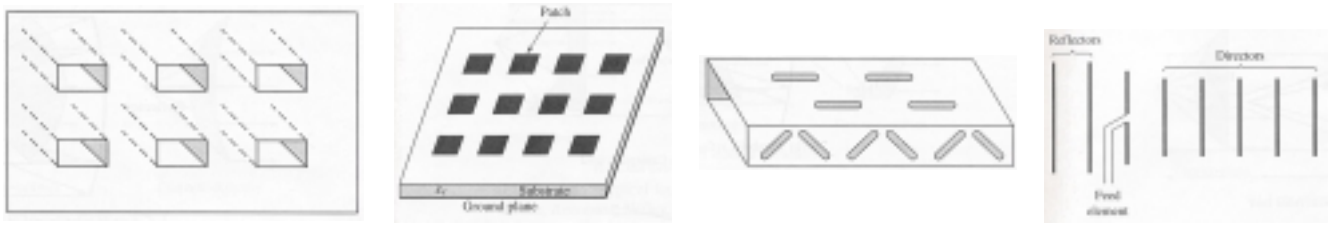
Pyramidal horn Conical horn Rectangular waveguide

Figure 32. Aperture antenna configurations [44].



Square Circular

Figure 33. Square and circular microstrip patch antennae [44].



Apeture array Microstrip patch array Slotted-waveguide array Yagi-Uda array

Figure 34. Typical wire, appeture, and microstrip array configurations [44].

5.1.1 Wire Antennae

Figure 31's wire dipole antennae come in various sizes and shapes depending on their target application. The radiation pattern of an antenna depends on its length, as illustrated in Figure 36. Figure 35 shows some commercially available pre-made wire antennae. These antennae are sometimes called whip-style, rubber-duck, or stub antennae. There are two main problems in obtaining a stub antenna: their connector and operational frequency. These antennae connect directly to the circuit's ground plane. Therefore, finding the right connector is important. Often stub antennae require reverse polarity subminature type A connector (SMA) or MMX or MX connectors that do not mate with standard SMA connectors. The second potential problem is finding a stub having the desired frequency range. Since DECT is a European band, it is challenging to locate commercially available stub antennae at 1.89 GHz in the US. Many of the readily available stubs are in the 2.3-2.5 GHz range. Fortunately, Centurion [45] makes quarter wave antennae at 1.850-1.970 GHz. For more information about antenna construction, consult [46].

Figure 35. Examples of commercially available quarter-wavelengh monopole antennae [46].

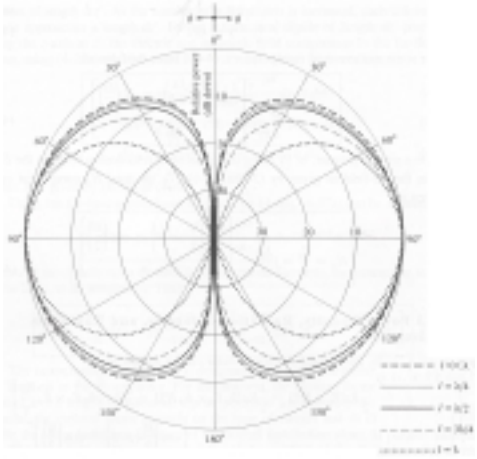


Figure 36. Radiation pattern of an antenna depends on its length [44].

5.1.2 *Microstrip Antennae*

Microstrip antennae consist of a conductive patch over a grounded substrate, as illustrated in Figure 33. The shape and size of the conductive patch determines the microstrip's radiation characteristics [44, 48, 49]. The conductive patch can be though of as a stripline that is used to drive the conductor's resonant mode [50, page 110].

A pico cell patch antenna is a microstrip antenna designed for indoor use. The term pico cell refers to the small radius of radiation. Unlike the omni directional wire antennae, the microstrip nature of the antenna makes its radiation pattern directional. Figure 37 illustrates the pico cell patch antenna, made by Smart Antenna and distributed by HD communications, chosen for this design. It has a 70 degree angle of radiation, Figure 37, and has a frequency range of 1.850-1.990 GHz. This project is designed to work with a microstrip antenna in case the wire antenna did not produce enough gain. While wire antennae usually give only 1.5-2 dBi[9] of gain, microstrip antennae usually give 8 dBi of gain.

Figure 37. Pico cell antenna [47].

5.1.3 *Typical Base Station Antennae*

For testing purposes and short range applications, the above antenna solutions make sense. Most base stations on the market need to receive and transmit signals over a larger area and require different antennae. These antennae are large, cost more than $500, and usually are suited for a large range of frequencies. Tessco is one company that sells these antennae [51]. They are designed to achieve maximum performance from a fixed or semi-permanent location. They are typically high-performance antennae such as gain Yagis, beams, and dishes [44, League., 2000 #4].

5.2 RF Filtering and Amplification

5.2.1 *RF Front End's Purpose*

Base station antennae often receive very weak signals whose bandwidth is much greater than the information bandwidth. The job of the analog RF front end is to provide initial band filtering and amplification. The requirement for band filtering just after the antenna is low insertion loss with a high Q-value dielectric resonator. Ceramic filters work well here. As was shown in the cascaded noise figure

[9] The Prefix Section: List of Terms and Abbreviations explains the concept of dBi.

analysis, in Section 4.3.1.4, the first amplifier's noise figure primarily effects the total noise figure of the circuit. Thus, low noise amplifiers (LNA) are chosen for the initial amplification.

Base station designs usually have two ceramic band pass filters (BPF) surrounding the LNA, as illustrated in Figure 15. The first BPF, located just after the antenna, performs initial band filtering and image suppression. Figure 18 and Figure 20 illustrate the concept of image suppression. The second BPF, located just after the LNA, provides further image suppression and attenuates any harmonics that are a result of amplification by the LNA.

5.2.2 Choosing the BPF

This design uses a ceramic filter from Murata designed for use in DECT applications. It has a 20 MHz pass band centered at 1.890 GHz. While my base station takes advantage of the pass band design in Murata's ceramic BPF, it can only partially utilize the maximum attenuation feature. Band pass ceramic filters are often designed so the maximum attenuation suppresses the system's image frequency. Image frequencies are illustrated in Figure 18, Section 0. The ceramic filter chosen for this design has a transfer function with maximum attenuation at 1.670 GHz, as shown in Figure 38. This design constraint is necessary because the BPF designers anticipated DECT applications to have an IF at 110.592 MHz, which creates an image frequency at 1.670 GHz. This design has an IF at 140 MHz, see Figure 16, which has an image at 1.610 GHz. Though the maximum attenuation feature is not fully utilized by this design, low-side injection still provides better image suppression than high-side injection as described in Section 6.1.1.

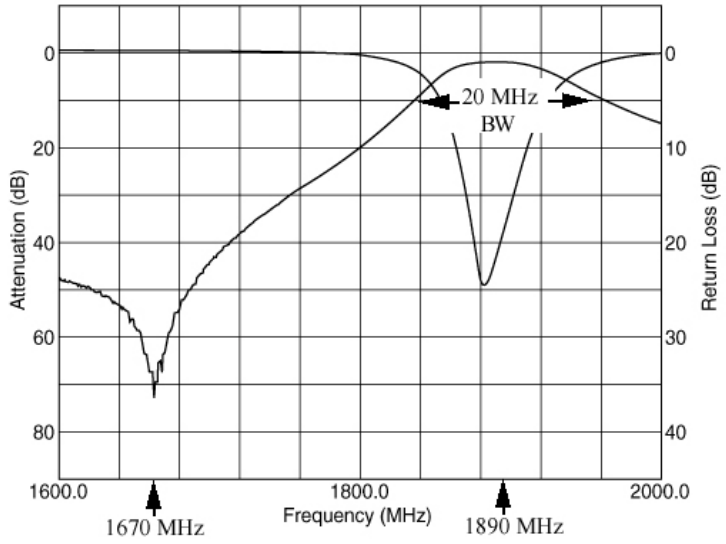


Figure 38. BPF's pass band is 20 MHz wide and maximum attenuation at 1.670 GHz [see 52].

5.2.3 Choosing the LNA

This design uses M/A-Comm's LNA because it has a gain of 14 dB, a noise figure of 1.4 dB, and an IIP3 of 18 dBm. In order for the LNA to perform at these specifications, the LNA must be carefully laid out and impedance matched. If either of these tasks are done poorly, unnecessary noise will be produced, causing signal degradation. This design implements the layout suggested by the BPF's and LNA's specification sheets. Figure 39 illustrates the LNA's suggested layout.

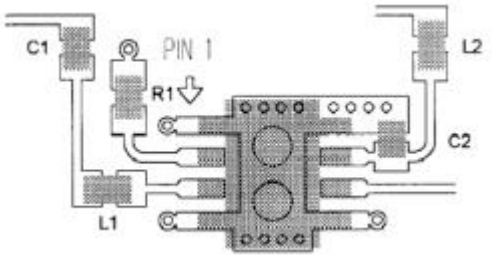


Figure 39. Recommended PCB layout for the LNA, [53].

If the layout is perfect and but the circuit is poorly impedance matched, signals will not pass through the RF block efficiently. The better impedance-matched the parts are, the less the signal is reflected back. Both paper Smith charts and computer aided matching programs were used to determine the proper matching network implemented. This network is diagrammed in Appendix B :Schematic. Since RF circuit simulation tools are not readily available, the values in the impedance matching network will have to be tweaked to match the particular board parasitics. Figure 98 illustrates how to set up the test equipment in order to perform the necessary "tweaking."

6 Downconversion

Given the limitation of the ADCs and the DSP/FPGAs currently available, the RF signal must be translated down to an intermediate frequency (IF). A mixer and a local oscillator are required to perform this needed frequency translation. Only after this translation, "downconversion," is performed, can the signal be digitized and the bits extracted.

6.1 Mixer

Mixers are a type of signal multiplier whose performance depends greatly on the way the multiplication is performed and the quality of the local oscillator.

6.1.1 Types of Signal Multipliers

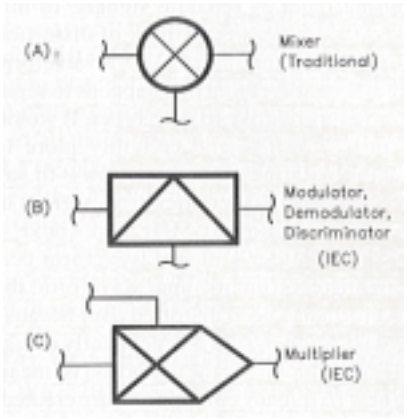


Figure 40. Three types of signal multipliers [17].

Mixers fall into the class of signal multipliers, devices that produce an output signal which is a function of the two input signals. There are three types of signal multipliers, as illustrated in Figure 40 . The first kind are called single-quadrant, two-quadrant or four-quadrant analog multipliers, according to the allowed signs of the operands.[10] Analog multipliers receive two signals and generate the linear product of their voltages. The second kind are modulators (sometimes called balanced-modulators[11], doubly-balanced modulators or high level mixers). Modulators can be thought of as sign-changers, since their function is to generate an output that is one input multiplied by the sign of the other input [18].

The third class of signal multipliers are mixers, which are optimized for frequency translation. Mixers have three ports: RF input, the local oscillator (LO) input, and IF output. An idealized mixer is

[10] For single-quadrant multipliers, both inputs must be unipolar; for two-quadrant multipliers, one of the inputs may be bipolar; in four-quadrant multipliers, both inputs may be bipolar [18].

[11] A good balanced modulator exhibits very high linearity with precisely equal gain for both positive and negative values of the inputs. These modulators generate an output which is simply one of the inputs multiplied by the sign of the other input. A good balanced modulator is a bad two-quadrant multiplier, for example, Motorola's MC1496 [54]. Balanced modulators are constructed so that the carrier is

shown in Figure 10. Transmitters use mixers to move a baseband signal up to an RF, modulating or upconverting it, while receivers use mixers to translate a signal down in frequency, demodulating or downconverting it. In a receiver, if the LO frequency is below the RF, the mixing process is called low-side injection. Alternatively, if the LO frequency is above the RF frequency, it is called high-side injection.

6.1.2 Image Frequencies

One solution that helps eliminate unwanted image frequencies, as described in Section 0, is to place an image-rejecting filter at the RF input, just before the mixer. This technique is used in this design. Another solution is to use a mixer that incorporates image suppression. The disadvantage to the second method is that these mixers consume more power than other mixer options since they require two mixer cells operating in quadrature [18].

6.1.3 Mixer Implementation

This design uses a downconverting Gallium Arsenide[12] (GaAs) monolithic microwave integrated circuit (MMIC) mixer with 8.5 dB single side band (SSB) noise figure, 9.0 conversion gain, and 0 dBm IIP3 from Hewlett-Packard [57]. The MMIC consists of a cascode FET structure that performs the basic mixing function, as shown in Figure 41. FET2 varies the transconductance of FET1 over a highly nonlinear region at the rate of the LO frequency [57]. The cascode structure inherently provides excellent LO-to-RF isolation, since there are two FET gates between the LO and the RF ports.

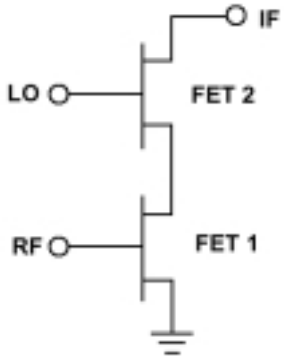


Figure 41. Cascode-connected pair of FETs make the mixer.

A good mixer is designed so that the IF and RF ports have a linear relationship. The 1-dB compression point and IIP3 define when the mixer's linearity breaks down. Once the system becomes nonlinear, say when RF increases by x dB, the IF will not also increase by x dB. The design incorporates a resistor between the source bypass pin and ground to increase the device current and, thereby, increase the mixer's linearity and output power. Graph 10 and Graph 11 illustrate how the device current effects the mixer's linearity (IIP3 point) and output power (P1).

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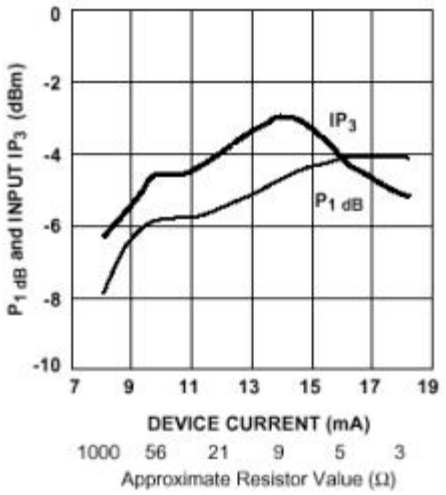
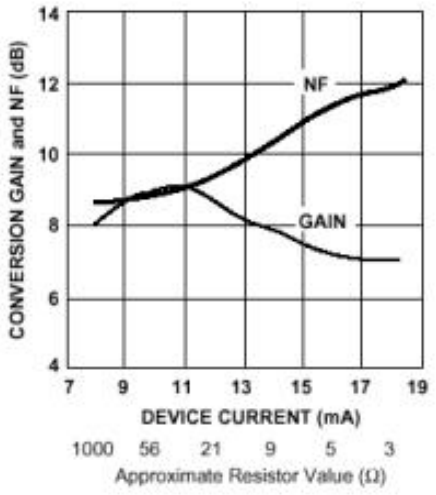
suppressed and any carrier noise is balanced out, i.e. the output only contains the sidebands. These are often used in AM transmission systems.



Graph 10. Mixer's 1-dB compression point and IIP3 vs. device current (resistor value) [57].



Graph 11. Conversion gain and noise floor vs. device current (resistor valude) [57].

Several design options can be considered to maximize performance of the downconverter: impedance matching, filtering, power supply connection, biasing current, bypassing, DC blocking, and layout. The RF and IF ports need to be impedance matched; the LO port is internally matched to 50 ohms. Figure 42 and Figure 43 illustrate the basic method of impedance matching using a Smith chart. Consult [58] for more examples of how to use a Smith chart for impedance matching. This design uses matching circuits that not only impedance match but also provide needed filtering, as in Figure 44 and Figure 45.

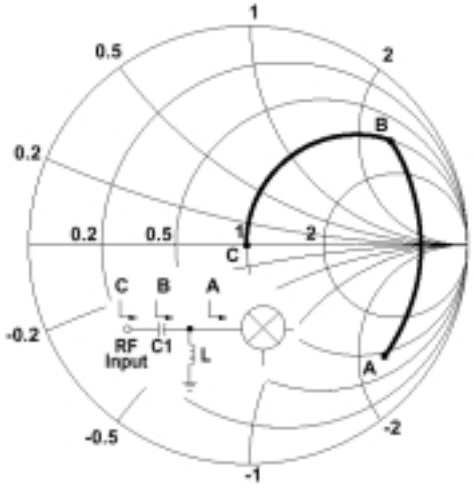


Figure 42. Smith chart used to impedance match the mixer's RF port [57].

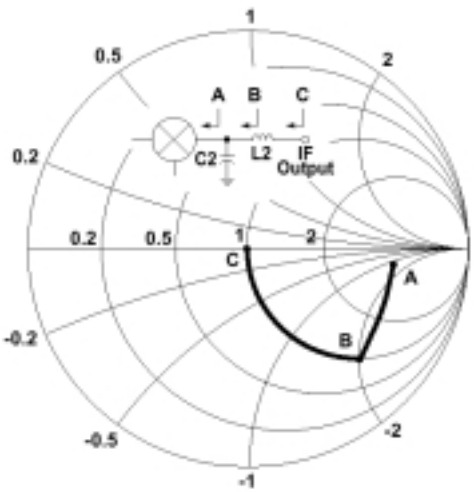


Figure 43. Smith chart used to impedance match the mixer's IF port [57].

[12] GaAs, silicon bipolar and BiCMOS technologies constitute the major section of the RF market. GaAs processes offer: higher breakdown voltages, higher cutoff frequencies, semi-insulating substrates, high quality inductors and capacitors [55, 56].

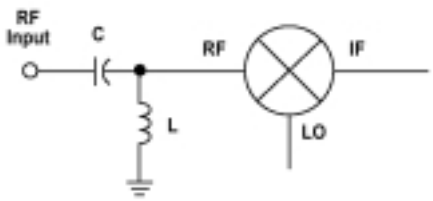


Figure 44. HPF architecture used for matching the mixer's RF port.

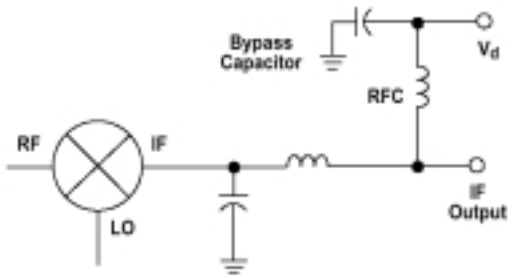


Figure 45. LPF architecture used for matching the mixer's IF port. Mixer is DC biased through the IF port.

Both the RF and IF ports handle their filtering constraints within their matching network. The RF port incorporates high pass filter characteristics into its matching network to eliminate interference from the image frequency. The impedance of the RF port is characterized by its reflection coefficient. Page 5 of the mixer's specification sheet [57] shows a list of reflection coefficients for different RF frequencies. The voltage reflection coefficient for the RF port, at 1.89GHz, has a magnitude of 0.82 and an angle of –37, and for the IF port it has a magnitude of 0.63 magnitude and an angle of –8 at 140 MHz. The gain from the RF to the IF port, at specified RF and LO frequencies, is called conversion gain. A well matched RF port can only increase the conversion gain by an amount equal to the mismatch loss. The mismatch loss is characterized by Equation (6.1). Therefore, the amount that impedance matching effects the overall conversion gain is a function of the reflection coefficient at the RF port. For a reflection coefficient, Γ_{RF}, of 0.82, the miss match loss, G_{RF}, is 4.847 dB. The IF port incorporates a low pass filter (LPF) into its matching network, to reflect RF and LO power back into the mixer, while allowing the IF signal to pass through. The 1.89 GHz frequency band is narrow enough to allow single frequency impedance matching.

$$G_{RF} := 10 \cdot \log\left[\frac{1}{1 - \left(\left|\Gamma_{RF}\right|\right)^2}\right] \qquad \textbf{(6.1)}$$

The mixer's power requirements are met by connecting the IF port to the analog power plane through the use of an inductor; see Figure 45. This inductor provides a way for DC biasing to enter the mixer through the IF port while still isolating the DC supply from any of the IF port's high frequency noise. Bypass capacitors keep the RF signal out of the power plane.

The mixer's biasing current is controlled with a resistor placed between the source bypass pin and ground. The amount of current that is allowed to flow through the device controls the IIP3, 1-dB compression point, noise figure, and mixer's conversion gain. Since the IIP3 point is a critical constraint

for this design, a value of 15 ohms is chosen for the resistor, placing the device current at 14 mA and the IIP3 at –3 dBm.

Bypassing and DC blocking are easily dealt with through the proper placement of properly chosen capacitors. Bypass caps placed between the IF port's power connection and ground shunt both low and high frequency noise currents to ground, preventing the IF signal from corrupting the analog power plane. DC blocking caps are placed before the mixer to prevent a DC voltage from hurting the mixer's performance. DC blocking caps are placed after the mixer to prevent the mixer from passing unwanted DC voltage levels to the rest of the circuit.

Mixer layout is another factor which influences downconversion performance. Layout can help minimize cross-talk between the three ports. This design implements the layout suggested in the mixer's specification sheet, shown in Figure 46. Multiple vias are used to reduce ground path inductance.

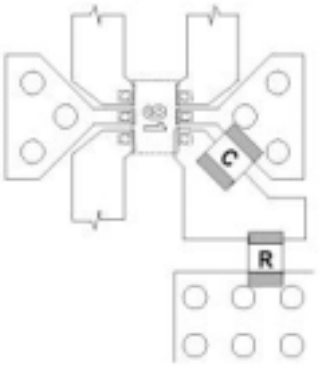


Figure 46. RF layout for mixer [57].

6.2 Frequency Synthesizer

The frequency synthesizer's function is to produce a stable frequency source for use as the mixer's local oscillator. This oscillator requires several parts as shown in Figure 47. The voltage controlled oscillator, VCO, needs an input voltage that is adjusted by a phased locked loop (PLL) to remain stable. The frequency synthesizer and loop filter produce this input voltage. The frequency synthesizer requires two components in order to produce this changing voltage. First, it needs a microcontroller that can, on system start up, program the synthesizer's dividers and, in effect, tell it how to control the VCO. Second, it needs a stable crystal oscillator that provides the reference phase to which the VCOs phase can be compared and locked.

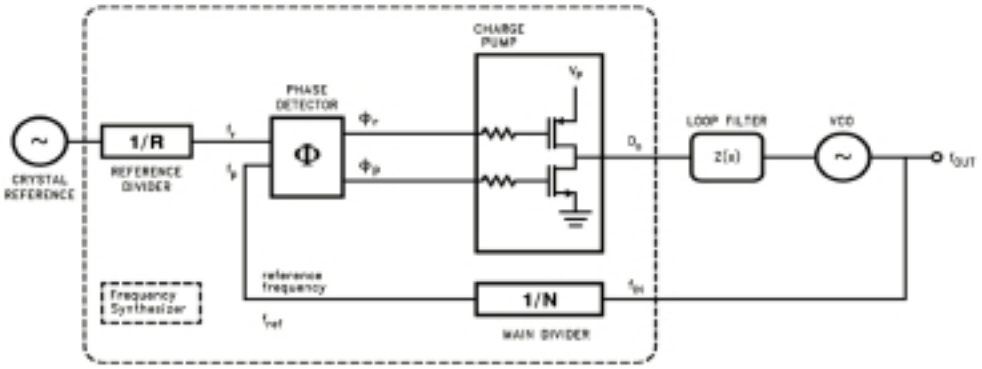


Figure 47. Basic charge pump PLL [59, pg 18].

6.2.1 Phased-Locked Loops

First, PLL theory is described. Then the various blocks that make up the PLL are discussed. Finally, the PLL mathematics are presented as an explanation of how and why the PLL works.

6.2.1.1 PLL Described

The basic principle behind and need for a PLL for local oscillator design is very simple. A spectrally pure, low jitter, low phase noise low frequency (LF) oscillator is easier to produce than a high frequency (HF) oscillator. In order to produce a high frequency source, a high frequency oscillator is designed and put into a feedback loop with a tuning system. The tuning system continuously compares the phase of the HF oscillator to a stable reference. The results of this comparison are used to steer the tuning and alternate the phase noise. Figure 48 shows the mechanism of a frequency synthesizer. The counter, which causes the loop to lock to higher harmonics of the reference oscillator, reloads to N whenever the count reaches 0 or 1, depending on the sequencer action..

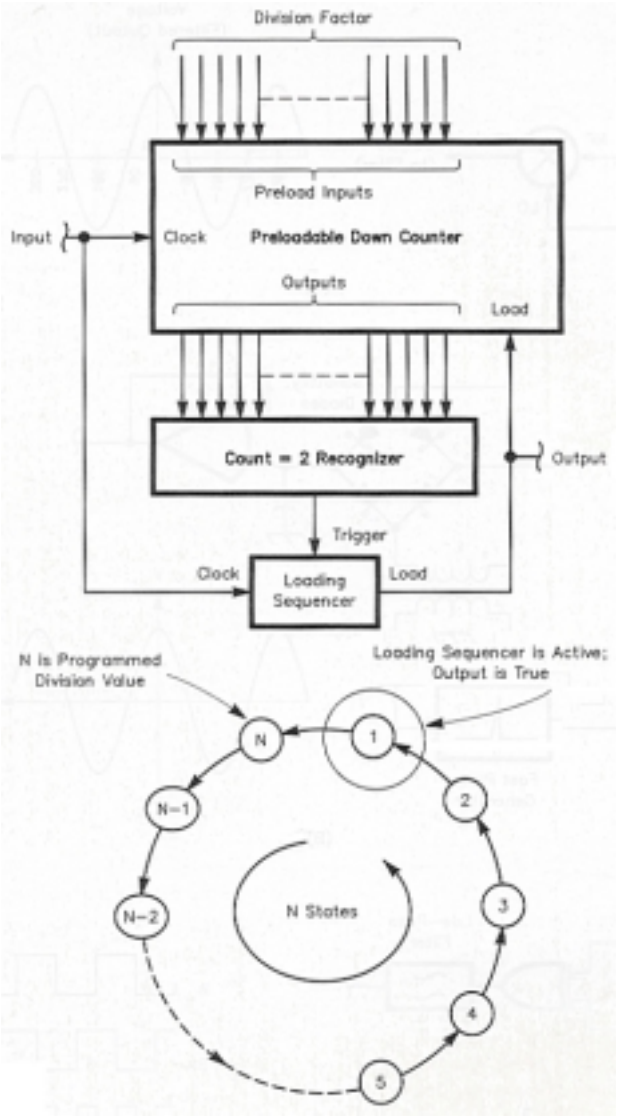


Figure 48. The mechanism of a frequency synthesizer [17, pg 14.37].

6.2.1.2 The Phase Detector and Dividers

Comparing the phase of two oscillators requires a phase detector (PD). A graphical example of this concept is presented in Figure 50. Here the PD's output pulse width is equal to the time difference between consecutive zero crossings of the two inputs. The DC output, V_{out}, of an ideal PD is linearly

proportional to the difference between the phases of the two inputs, $\Delta\phi$, as illustrated in Figure 49. This DC output, after passing through a LPF, controls the frequency and phase of the VCO.

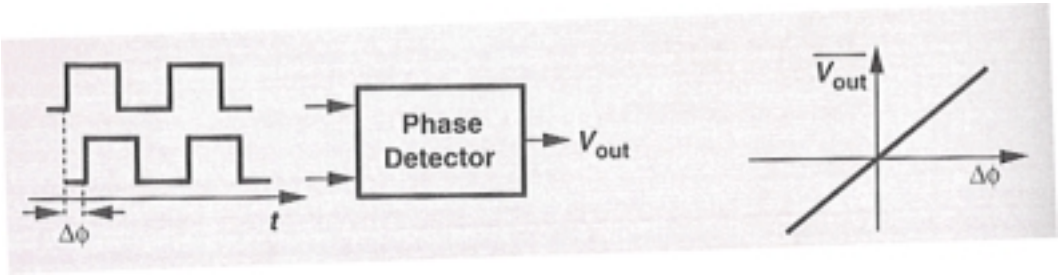


Figure 49. Illustration of an ideal phase detector [43, pg 250].

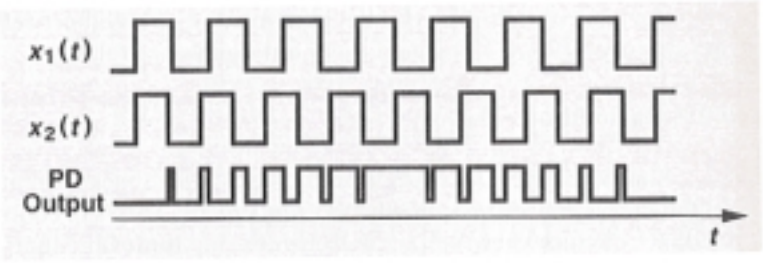


Figure 50. PD's input and output waveforms [43, pg 251].

The output of the VCO feeds back into the phase detector. The VCOs output and the reference oscillator pass through dividers before reaching the phase detector. This step allows the phase detector to operate at a lower frequency that is a sub multiple of both frequencies. The HF oscillator's divider is usually called the main divider, while the LF oscillator's divider is called the reference divider. Figure 47 is diagram of these dividers and their relationship to the PLL.

Equation (6.2) illustrates the numerical relationship between the output frequency (f_{out}), reference oscillator (f_{ref}), phase detector (f_{pd}), reference divider (R) and main divider (N). This project's detector operates at 1.75 GHz/525 = 30 MHz/9 = 3.333 MHz, as illustrated in Figure 17. The phase detector, and thus the frequency synthesizer that contains the phase detector, is capable of tuning in unit intervals of f_{ref}/R.

$$f_{pd} := \left(\frac{f_{out}}{N} := \frac{f_{ref}}{R} \right) \qquad \textbf{(6.2)}$$

To deal with GHz frequency division, the main divider would need to be built from ECL devices. This option would be very expensive and power costly. Programmable frequency synthesizer main dividers have a fast front end divider called a prescaler; see Figure 51. The prescaler is capable of fast division of the high frequency signals, allowing the main divider to deal with an already divided signal.

Figure 52 shows how this prescaler works. These prescalers are also called dual-modulus prescalers. Since the prescaler must go through x number of states, there is a minimum division ratio. Consult [17, pg 14.33-14.45] and [59] for a complete picture of dual-modulus prescalers.

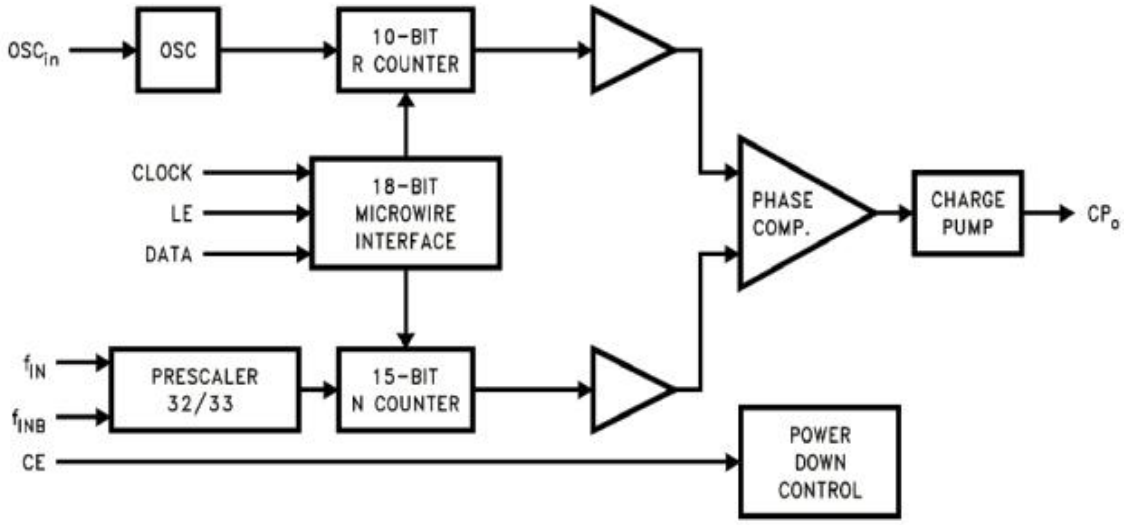


Figure 51. LMX2324 2.0 GHz Frequency synthesizer's block diagram [60].

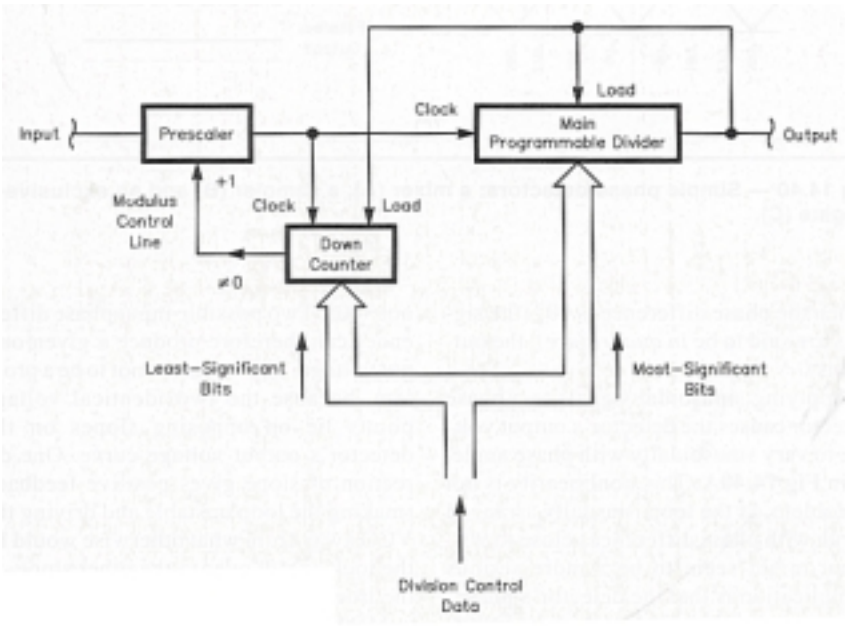


Figure 52. Functional block diagram of a dual-modulus prescaler [17, pg 14.37].

6.2.1.3 The Loop Filter and the Charge Pump

The phase detector operates at a frequency set by the frequency step size. An ideal phase detector only outputs the phase error voltage, but, in reality, phase detectors also output the frequency

step size and its harmonics. A low pass filter, called the "loop filter," is placed between the PD and the VCO to filter out these unwanted frequencies.

Some loop filters also average the PD output by depositing charge onto a capacitor during each phase comparison and allowing the charge to decay afterwards. This process takes time. If a charge pump is placed between the PD and the LPF, there is negligible delay between the phase comparisons by the PD and error voltages reaching the VCO. Figure 47 illustrates the location of this charge pump. Since this design needs the IF signal to be as clean as possible, it is important to have a frequency accurate local oscillator source for the mixer. Therefore, a frequency synthesizer that has a charge pump was chosen to increase the frequency accuracy of the LO; see Section 6.2.2 for further discussion on frequency accuracy and update time.

6.2.1.4 The Reference Oscillator and the VCO

Since the goal of the PLL is to produce a stable, accurate frequency source to be the mixer's local oscillator (LO), the question might be asked, why not just use a regular oscillator. Regular oscillators, designed to be the clocks of noisy digital circuits, do not meet the phase noise requirement imposed by an IF sampling receiver. The most frequency-stable, highest Q oscillators are oscillators that use the fundamental frequency of the crystal resonator. To produce a higher frequency, like the 1.75 GHz LO needed, the oscillator would need to use a multiplier. This multiplier would amplify any phase noise of the original quartz resonator. Unlike IF sampling receivers, most digital circuits can still operate with plenty of phase noise. But using an oscillator with a multiplier as the LO of a mixer would mean that the quartz resonator would have to meet an even stricter phase noise requirement.

A better, and realistic, solution is to use a VCO[13] in a PLL. VCOs produce relatively stable frequency outputs, but they drift somewhat. Putting the VCO in a PLL with the low phase noise crystal resonator allows the VCOs phase to lock with the crystal's phase, insuring stability. This technique utilizes the good parts of both the crystal and the VCO.

6.2.1.5 PLL Mathematics

All of the above blocks, a phase detector, main divider, reference divider, charge pump, VCO, and reference oscillator, fit together to form a phase-lock loop feedback system shown in Figure 47. A

[13] While current controlled oscillators might be a choice for a GHz oscillator, it is difficult to produce high-Q storage elements whose value can be controlled with a current [43].

mathematical model of the PLL must be created before the parameters that cause phase noise and spectral output can be determined. Figure 53 shows a linear control system model of a phase feedback loop.

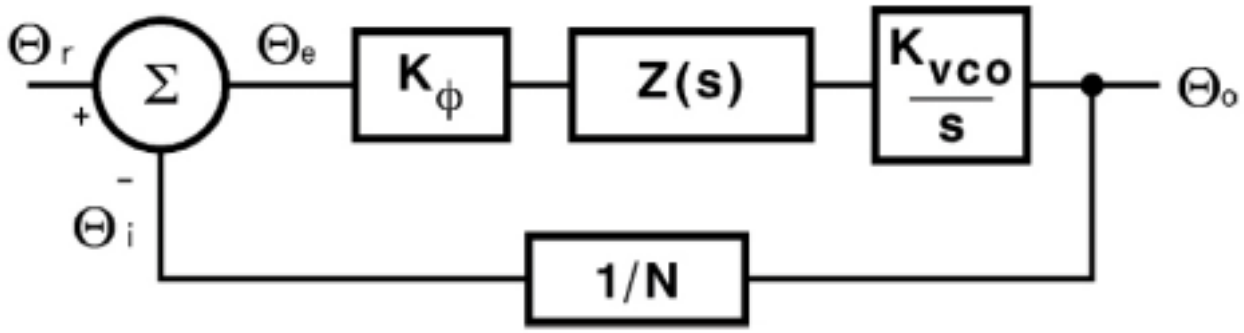


Figure 53. Linear mathematical model of a PLL [59].

From control theory, the open loop transfer function of the system in Figure 53, (Θ_i/Θ_e where Θ_r is the reference oscillator's phase, Θ_e is the error voltage's phase, Θ_I), is Equation (6.3), is the divided VCOs phase, K_ϕ is the phase detector gain, K_{VCO}/s is the VCO gain, Z(s) is the loop filter gain, and N is the gain of the feedback counter modulus.

$$H(s)\cdot G(s) := \frac{K_\phi \cdot Z(s)\cdot K_{VCO}}{N\cdot s} \qquad \textbf{(6.3)}$$

The resonant frequency, ω_r, and the 3 dB bandwidth of this transfer function relate to the speed of the transient response [61, page 440-443]. In a phase lock loop, this speed is the "locking" speed. Therefore, the next step to understating the trade-offs in designing a PLL is to determine the open loop bandwidth of this transfer function. Generally, the narrower the loop bandwidth, the lower the reference spurs and the longer the lock time. Consult [59, 61] for a more thorough explanation of the subject.

The VCOs phase is locked with the crystal phase through the use of a control voltage. The following equations give a feel for what conditions must be met in order for the PLLs output to have the desired spectral content. The control voltage dictates when and how much the VCO adjusts the frequency of the previously outputted frequency signal. If this control voltage is a sinusoidal modulation,

$$v_{cont}(t) := V_m\cdot\cos\left(\omega_m\cdot t\right),$$

then the PLLs output is

$$y(t) := A\cdot\cos\left(\omega_{FR}\cdot t + \frac{K_{VCO}}{\omega_m}\cdot V_m\cdot\sin\left(\omega_m\cdot t\right)\right),$$

where ω_{FR} is resonant frequency of the transfer function. If the system is an FM narrowband system, like the one in this design, where

$$\left| \frac{K_{VCO} \cdot V_m}{\omega_m} \right| < 1,$$

then the output spectrum of the PLL will only be a main component of ω_{FR}, with side bands at $\omega_{FR} \pm \omega_m$.

It is interesting to note that the key requirements for a VCO usually include spectral purity, linear voltage-to-frequency transfer characteristics, and good frequency stability as either the power supply or the temperature changes [62-64]. For base station applications, the VCOs long term frequency stability specification is not a concern, as long as the rate of change of the frequency drift is still within the PLLs bandwidth[14].

6.2.2 PLL Figures of Merit

While a tight tolerance in frequency is achieved by phase locking the VCO to a crystal through the use of a PLL, there remain some problems with PLLs. These problems are quantified by the following PLL figures of merit: phase noise, spurious output, lock time

6.2.2.1 Phase Noise

Phase noise is a measure of the spectral purity of the tone produced by the PLL. While the noise characteristics of the reference oscillator, VCO, and dividers directly effect the spectral purity of the tone, the critical issue that effects phase noise is the reference oscillator's specifications. Any phase noise on the reference oscillator directly effects the phase noise of the PLLs output frequency. Phase noise is measured in dBc/Hz[15] and is the ratio of single side band power to the total carrier power. The side band power is measured within 1 Hz bandwidth at a pre-defined offset frequency.

6.2.2.2 Spurious Output

Ideal phase detectors only output the steering signal (the error correction voltage). Since the phase detector compares the two oscillator's phases at F_{ref}/M, in reality, phase detectors also output

[14] It is interesting to note that for low power transmitters, the important VCO properties reduce to just spectral purity, high operating frequencies maintaining low power consumption, and small size factor. High linearity and wide tuning ranges are not important specifications, since most wireless applications have bandwidths limited to a few tens of MHz.

F_{ref}/M and the F_{ref}/M's harmonics. Since HF oscillators, such as the VCO, are extremely sensitive, the loop filter must block these unwanted frequencies. Though most loop filters have a LPF to filter out the F_{ref}/M signal, some of the F_{ref}/M signal always reaches the VCO. This explains why the output frequency spectrum of any PLL has side bands spaced at a distance equal to the phase detector's operating frequency (F_{ref}/M) (and harmonics) away from the carrier. These side bands are called reference frequency side bands or reference spurs and are graphically illustrated in Figure 54.

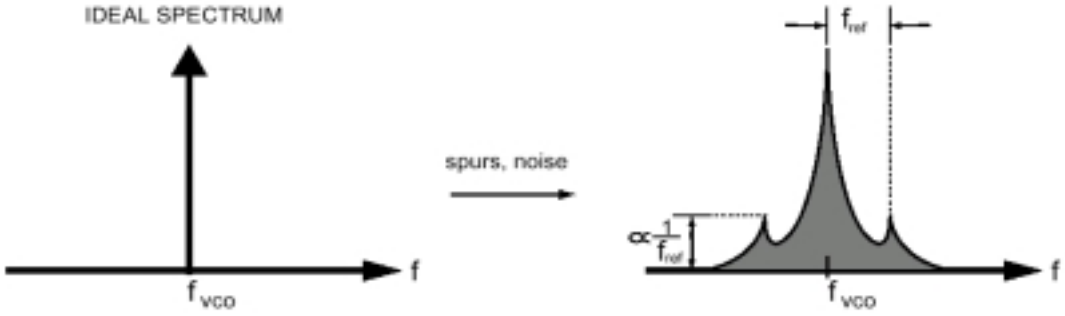


Figure 54. Illustration of reference spurs [23].

6.2.2.3 Lock Time

Lock time, or switching speed, measures the settling time of the PLL once a change in frequency has been initiated by the phase detector. The system is "locked" once the system outputs a signal whose frequency accuracy satisfies the design. Therefore, it only makes sense to consider lock time once the frequency accuracy and frequency step size are determined.

The accuracy of the frequency output of the PLL depends on how quickly the error voltage generated by the phase detector is fed back to the VCO. If frequency accuracy is the primary concern for the local oscillator, the error voltage should be fed back to the VCO as quickly as possible. The benefit of fast feedback is that any frequency drift from the VCO will be corrected quickly. The downside is that it creates an increase of electrically generated noise. This noise has two causes, the first of which is called overshoot. When the VCOs frequency drifts up slightly, an error voltage is created that brings the frequency back down. If this error voltage overcorrects and reduces the frequency too much, then it must correct again, pushing the signal's frequency up, etc. This phenomenon is called overshoot. Constant "nudges" from the error voltage cause excess current to flow into the circuit, creating the 2nd type of noise.

On the other hand, if low noise output is of paramount concern, the PLL should allow the VCO to drift for a longer time, reducing the number of times the error voltage must be created in order to

[15] The Prefix Section: List of Terms and Abbreviations explains the concept of dBc.

change the VCOs output frequency. Longer drift time means the output frequency will deviate more greatly from the desired frequency output, but sending error voltage correction less frequently often minimizes the amount of electrical noise created [65].

6.2.2.4 Board Interference

The layout of the individual PLL components, placement of the PLL block, and shielding of the PLL block on an RF circuit board is critical for the proper operation of the PLL itself and the proper operation of the RF circuitry around the PLL. Appendix C: Board Layout illustrates how this design implements the layouts suggested by the VCOs specification sheet and the frequency synthesizer's evaluation board [59].

The PLL needs to be located on the RF board in a space that is as close as possible to the mixer, but still allows for adequate shielding. Shielding of the PLL block is essential since the PLL has both oscillators and digital components. The VCO and the reference oscillator both create unwanted harmonics that can easily corrupt RF signals if left unshielded. The frequency synthesizer and microcontroller are digital parts that have the potential of likewise dirtying the power and ground layers. Appendix C: Board Layout illustrates how shielding is placed around the PLL parts to limit the amount of noise generated by the PLL that enters the RF circuitry.

Grounding the PLLs components properly is also critical to the functionality of the PLL and the way the PLL components interfere with the power and ground planes. Section 8.4 outlines the grounding method for the RF and digital boards. The VCO must be attached to the RF ground plane and not the digital ground plane. The VCO requires a clean ground since any noise on the ground pins directly translates into frequency noise at the VCOs output. For example, if the VCO is modulated at 100 MHz/V and there is 10 mV of ground noise, this will produce a 1 MHz frequency swing in the VCOs output. On the other hand, the microcontroller must be connected to the digital ground plane since, being a digital component, it produces a lot of ground noise and can tolerate the dirty ground plane. The frequency synthesizer has to be connected to both the RF and the digital ground plane. All ground pins and bypass capacitors should be connected to a clean analog ground plane, while the charge pump and MICROWIRE circuit’s grounds can be connected to the digital ground plane.

6.2.3 Programming the Frequency Synthesizer

The frequency synthesizer needs the reference divider values and the main divider values upon system start-up. The particular frequency synthesizer chosen for a design effects the calculation of these

numbers. For this design, a National Semiconductor PLLatinum Frequency Synthesizer, LMX2324 [60], is chosen.

On system start up, the frequency synthesizer's Programmable Reference Divider (R Counter), Prescaller Select (S Latch), and the Programmable Divider (N Counter) need to be configured. With the guidance of Application Note 1098 from National Semiconductor [66], a microcontroller is employed to program the frequency synthesizer on start up. This design uses the COP8SAA718Q9 microcontroller from National Semiconductor. This microcontroller uses a MIRCOWIRE serial interface for data communication. MICROWIRE is a three wire, serial input, serial output, and serial clock, bi-directional serial synchronous communication protocol; see Figure 55, and National Semiconductor's Application Note 579 [67] for a more detailed description of this communication protocol.

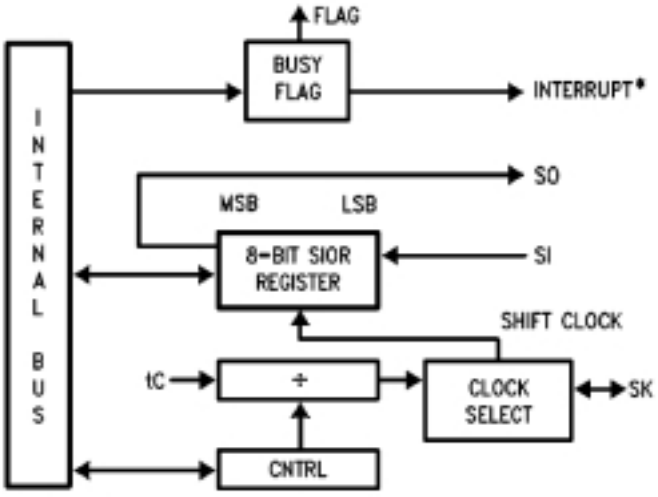


Figure 55. MICROWIRE protocol [67].

The design parameters for the microcontroller are as follows:

1. Configure the following registers: the Programmable Reference Divider (R Counter), the Prescaler Select (S Latch) and the Programmable Divider (N Counter)
2. Organize the configuration data into "data streams" according to the specified protocol sequence outline in the frequency synthesizer's specification sheet.
3. Pad data streams with leading zeros if necessary.
4. Control the Load Enable (LE) signal of the frequency sync
5. Generate a clocking source.
6. Place the microcontroller into a power down mode, allowing it to draw virtually zero current.
7. Have a diagnostic mode that tells the programmer if data has been sent to the frequency synthesizer for debugging purposes.

The microcontroller, being a digital part, can produce high levels of noise on the analog power and ground planes. Therefore, design parameter 6 is critical for minimizing noise during system

operation. The connections between the microcontroller and the frequency synthesizer, including the DEBUG LED, are shown in Figure 56. The timing interface between the microcontroller and the frequency synthesizer is shown in Figure 57. The code for this project is an implementation of the flow chart shown in Figure 58.

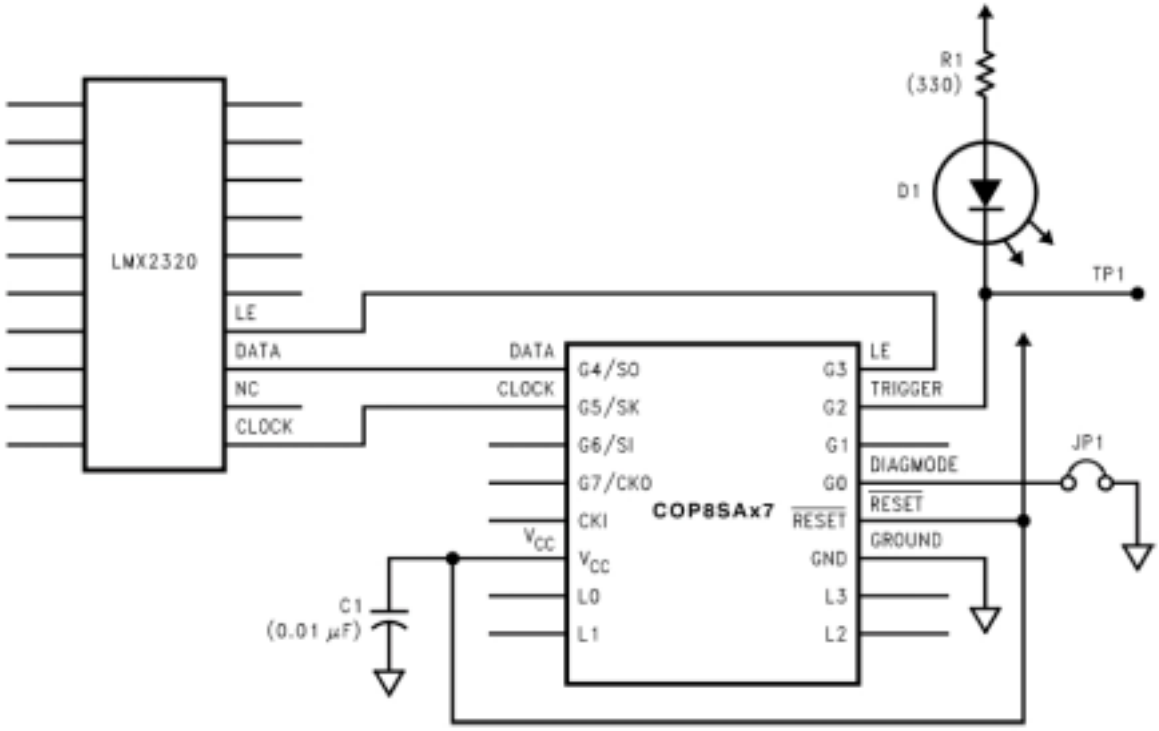


Figure 56. Connections between the microcontroller and the frequency synthesizer [67].

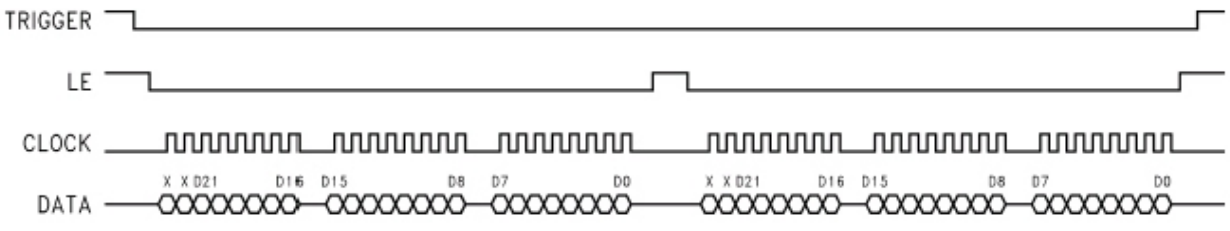


Figure 57. Timing diagram of programming the frequency synthesizer on system start-up [67].

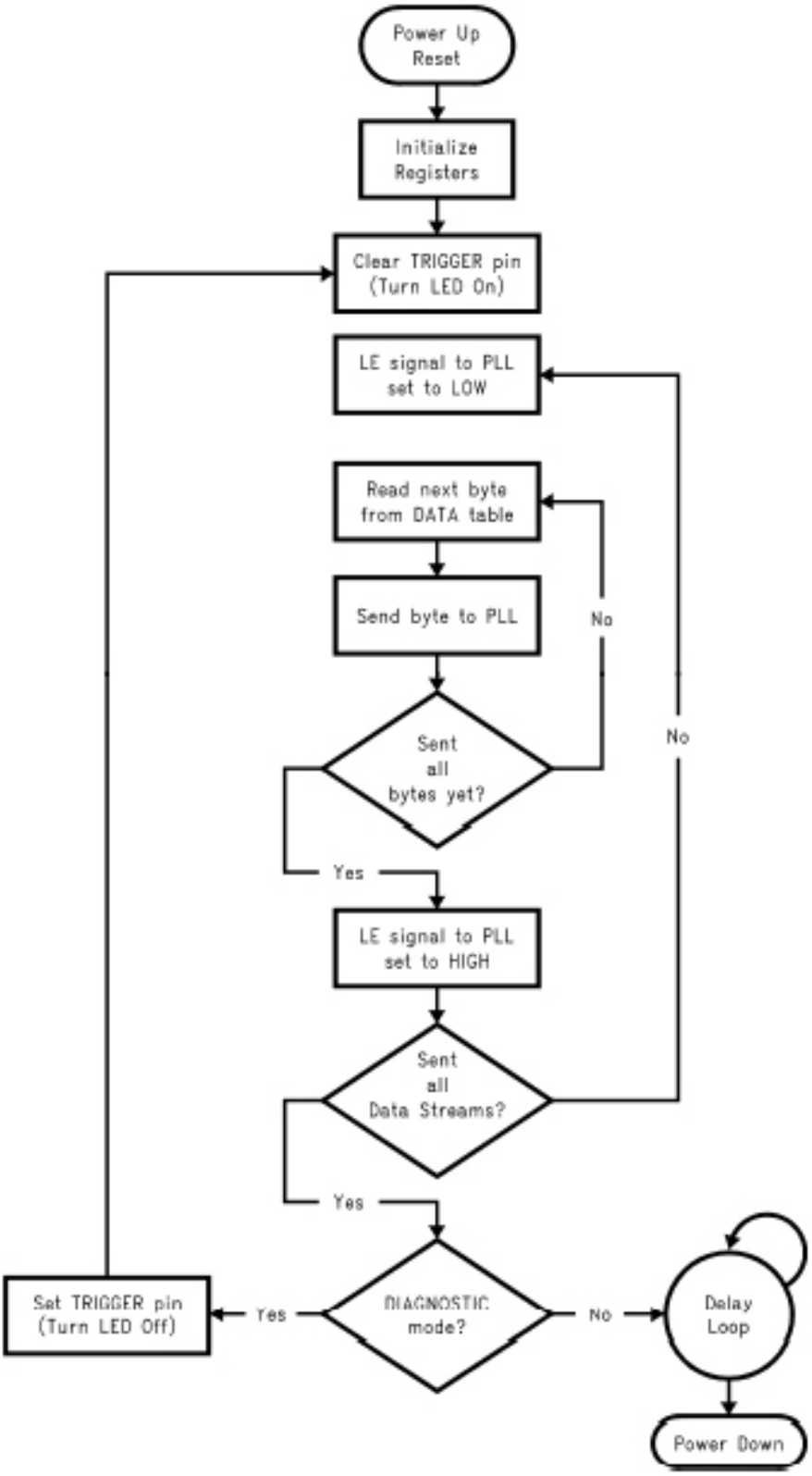


Figure 58. Flow chart illustrating connection between the microcontroller and the frequency synthesizer [67].

6.3 IF Filtering

The IF signal is bandlimited by a SAW before any further amplification is performed. Band limiting reduces the amount of noise that gets carried down through the signal path. While the filters in the RF path were 20 MHz wide, the SAW needs to be just wider than the bandwidth of the signal. Because the signal is a 2.5 Mbps GFSK signal with a BT of 0.5, it takes up 3.325 MHz of bandwidth. Therefore, the SAW filter needs to be slightly greater than 3.325 MHz, but not so wide that, when the signal is subsampled, the aliased copies interfere with one another. The 4 MHz SAW filter from Sawtek [29] was chosen because of its physical properties, availability and filter characteristics.

The advantages of using a SAW filter are derived from their rugged, reliable physical structure. Their operating frequencies are set by a photolithographic processes, which means they don't require complicated tuning operations. The physical designs of the SAW devices are illustrated in Figure 59 and Figure 60.

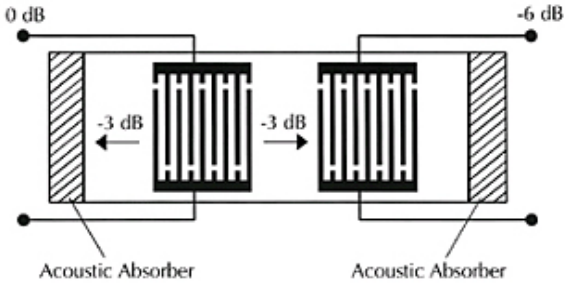


Figure 59. Simple trasversal SAW filter configuration [27].

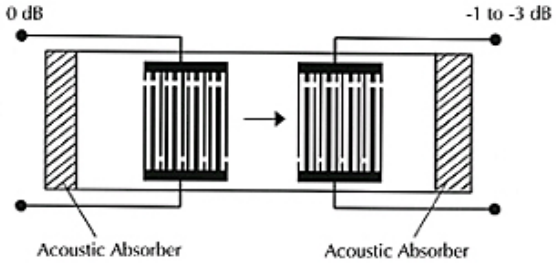


Figure 60. Single-phase unidirectional filter configuration [27].

The IF Amplifier requires a dual ended signal. This design capitalizes on the SAW's ability to turn a single ended (SE) signal into an isolated dual ended (DE) signal.

Proper impedance matching and board layout effect the SAW's ability to perform. This design implemented the recommended layout from the SAW's specification sheet, Figure 61, and the layout from the IF Amplifier's demo board.

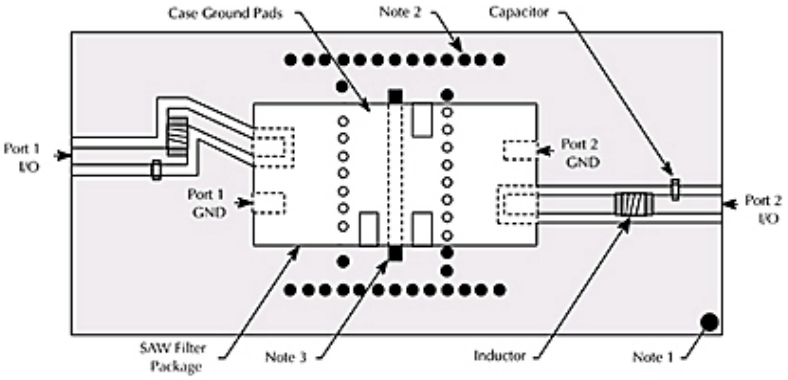


Figure 61. Optimal PCB layout for SAW filter [27].

7 Sampling Clock Requirements

ADC sampling clock jitter is a dynamic specification critical to the performance of a software radio. The primary effect of sampling jitter on system level performance is the degradation of the SNR. While jitter effects base band performance, the effects of sampling jitter are magnified by high frequencies. The degree of degradation is directly proportional to the frequency of the IF signal when sampled by the ADC. Often, the effect of jitter on undersampled signals is misunderstood. Therefore, understanding the causes of jitter, its mathematical representation, and its effect on the system performance are essential to correctly specify the performance required of a sampling clock. Over-specifying the jitter requirement can cost the developer valuable time and money. With the increase in popularity of IF sampling base stations, low jitter (1 psec to 50 psec) sampling clocks currently have a 32 week lead time. Even if the design can wait the allotted lead time, low jitter sampling clocks can typically only be ordered in large quantities.

7.1.1 Oscillator Jitter Origins

The location of the clock edges in Figure 62 vary randomly with time. The noise that causes this random variation can be quantified by its power or degree of spectral content. It is critical to remember that the spectral content of clock jitter differs greatly depending on the clock-generation technique used [1]. Since there are a number of different oscillators commercially available, see [68], understanding the causes of jitter allows the designer to know what to look for when selecting an oscillator. The structural, and therefore behavioral, properties of a crystal resonator influence the accuracy of the oscillator. The spectral content of the noise on the oscillator's output feeds into the ADC, effecting the ADC's ability to sample accurately, thereby effecting the base station's ability to reconstruct an undersampled signal. Therefore, jitter from the crystal resonator and the oscillator increases the base station's BER.

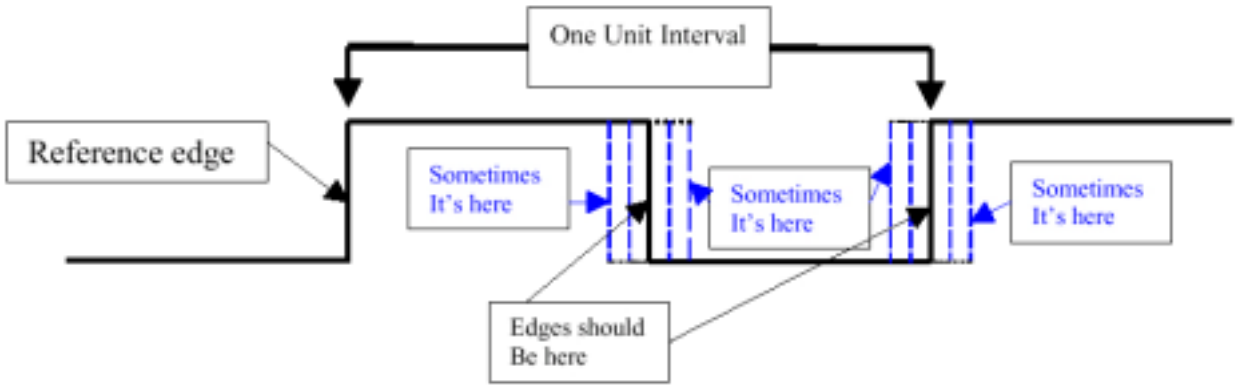


Figure 62. Digital waveform with jittered edges [69].

7.1.1.1 Quartz Crystal Resonance

The piezoelectric properties of a crystal allow it to perform like a resonator. Figure 63 shows how mechanical strain produces electrical polarization, and how electrical polarization produces mechanical strain in piezoelectric materials. In other words, a voltage produces stress on the crystal and an alternating voltage, applied at a the crystal's resonant frequency, causes the crystal to vibrate. This vibration creates a steady signal at the output of the oscillator. So, the crystal's vibration accuracy, and its modes of vibration, determine the oscillator's output signal. Therefore, the crystal's properties directly effect the oscillator's frequency stability, which, in turn, effect the ADC's sampling accuracy and the base station's BER.

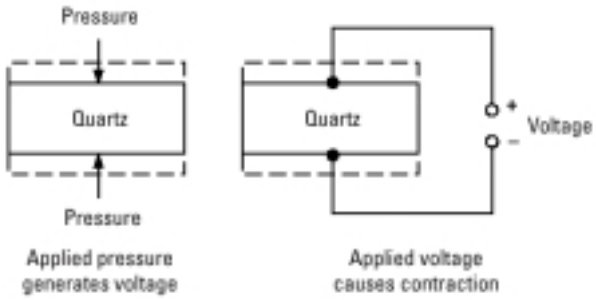


Figure 63. Piezoelectric properties of crystal [68].

A crystal's piezoelectric coefficients are a function of the crystal's physical structure. The physical structure is determined as the crystal grows. Imperfections in the growth of the crystal will cause the crystal to have poor resonating properties, making it unsuitable for an oscillator reference unit. The resonance of a crystal produces an oscillation frequency when it is suitably located in a feedback loop around an amplifier. Therefore, the more regular the crystal structure, the better it is at resonating, minimizing jitter.

7.1.1.2 Importance of the Quartz Crystal's Cut

The piezoelectric coefficient determines the crystal's ability to resonate and produce a frequency. Even if an oscillator manufacturer uses a crystal with perfect regularity in the structure, the process of

taking a raw, regular structure crystal and turning it into a useable quartz resonator involves great craftsmanship. The piezoelectric properties of a crystal are highly sensitive to the cut and thickness of the quartz resonator. A considerable amount of work is required to extract a quartz resonator from a raw crystal.

The extraction process is performed with careful consideration toward the cut axis and thickness. These choices determine the physical and electrical parameters of the resonator. Figure 64 illustrates the relationship between the axis for cutting and the physical and electrical parameters of the resonator. The choice of axis with which the crystal is cut, as shown in Figure 65, determines the mode of vibration: thickness sheer[16], face shear, or extensional. For example, the X cut vibrates in an extensional mode, whereas a cut 35 degrees off the Y axis exhibits a thickness shear vibrational mode. The cut axis also can determine if the feedback loop produces harmonic or nonharmonic signals and overtones. While harmonic overtones allow the crystal the capability of producing higher frequencies than its fundamental resonating mode, nonharmonic overtones can cause the crystal to shift from one resonant point to another, thus producing an undesirable frequency jump.

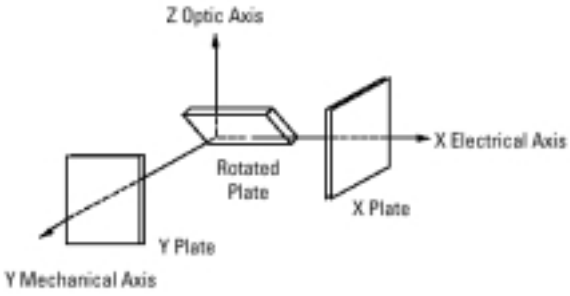


Figure 64. Choice of axis and angles to cut crystal [68].

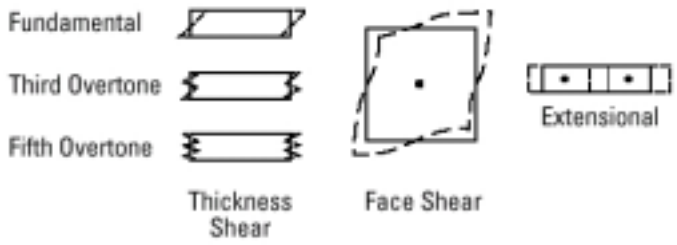


Figure 65. Crystal cut and thickness sheer determine vibration modes [68].

The rate of vibration, the signal's center frequency, and spectral purity is determined by the cut, size, and shape of the resonator. For crystals operating in the thickness sheer vibrational mode, and for crystals with the AT and BT cuts, as shown in Figure 66, the center frequency is determined by the thickness of the cut. The consistency of radius of curvature of circular crystals determines the spectral purity of the frequency. Crystals with smooth curvature produce "clean" frequency outputs with no spurious tones.

[16] Webster's dictionary defines shear as: "the lateral deformation produced in a body by an external force, expressed as the ratio of the lateral displacement between two points lying in parallel planes to the vertical distance between the planes."

In essence, high performance oscillators, fundamental to the design and implementation of SDR, require high quality quartz resonators.

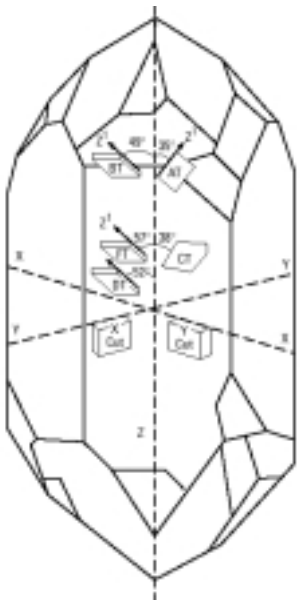


Figure 66. Doubly terminated quartz crystal's typical axis cuts [68].

7.1.1.3 Electrically Modeling the Quartz Crystal's Physical Properties

Once the quartz's axis, size, and shape are determined and the cut is performed and verified[17], the electrical-mechanical capabilities and the thermal capabilities of the crystal are set. Therefore, a mathematical model of the quartz can be constructed to allow the oscillator manufacturer to determine the type of feedback loop in which to put the quartz. Figure 67 shows how a quartz resonator can be modeled as a capacitor and inductor in series. R_1 is a result of bulk losses, C_1 is the motional capacitance, L_1 is determined by the mass, and C_0 is made up of the electrodes, holder, and leads. Figure 69 illustrates the mounting options that effect C_0. The circuit in Figure 67 reduces to either a capacitor, resistor, inductor, or some combination of them, depending on the frequency sent to the quartz resonator, as illustrated in Figure 68

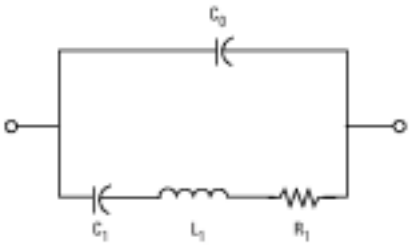


Figure 67. Electrical model for quartz resonator [68].

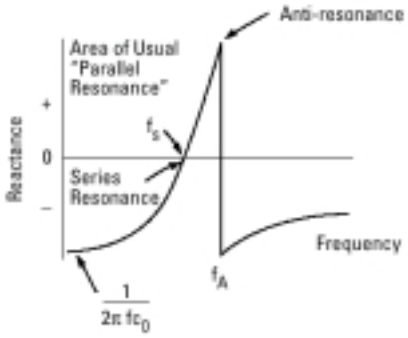


Figure 68. How a crystal's reactance varies with frequency [68].

Figure 69. Various mounting techniques and packages [68].

[17] Polarized light, X-rays, and chemical etching are some of the techniques used to detect the presence of defects.

7.1.1.4 Quartz Crystals in a Feedback Loop

To utilize their piezoelectric properties, quartz resonators are used as a frequency source by placing them in a positive feedback loop, as can be seen in Figure 70. This method allows the mechanical vibrations and changing voltages to feed back on each other and produce a very stable frequency. Figure 70 shows how placing this quartz resonator into a feedback loop with an amplifier accomplishes this task and causes the quartz resonator to act like a tuned circuit. In this configuration, a small amount of energy is fed back into the crystal, causing the crystal to vibrate at a resonance frequency. The resonance value is the frequency generated by the oscillator circuit.

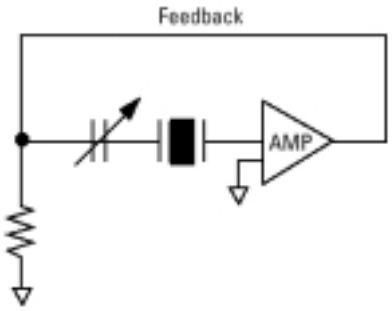


Figure 70. Simple oscillator feedback circuit using a quartz resonator [68].

The level of amplification in the feedback loop determines the amount of jitter present in the output. If a quartz resonator has 5 ps of jitter and is placed in a feedback loop with amplification of 10, the output will have 50 ps of jitter. If this same quartz resonator is placed in two oscillators, the oscillator without a gain multiplier, (having amplification equal to 1), has less jitter than the oscillator that uses a gain multiplier, (having feedback loops with amplification greater than 1).

For this reason, SDR will have the best BER if their sampling frequency matches the fundamental frequency of a quartz resonator exactly. The task for a SDR engineer trying to minimize BER is to design the base station to use an oscillator that operates at the fundamental frequency of a quartz resonator. Since the demand for low jitter clocks far outweighs the supply[18], the limiting factor in undersampling base station design is the acquisition of a low jitter clock.

The first SDR design challenge is to find a manufacturer who uses high-performance quartz resonators in their oscillators. The next step is to determine which of the oscillator frequency selections are produced without a multiplier. The final, most critical step is to discover which of these oscillators operating in the fundamental mode of the quartz resonator are available for purchase.

The sampling frequency is then selected amongst only a few options of available low jitter clocks that ALSO meet the sampling requirements of the system. This design chooses a 16 MHz sampling clock

[18] Oscillator manufactures obtain their crystals from a mine. The supply of superior crystals has decreased due to the sharp increase in applications requiring low jitter clock sources. Thus, the lead time for obtaining a low jitter clock can now run anywhere from 30 to 60 weeks to "we are unable to specify a delivery date at this time."

with 38 ps max jitter[19]. After establishing the sampling frequency, the engineer can finalize the IF frequency location choice and determine the demodulation method needed.

7.1.2 Oscillator Frequency Stability

Frequency stability has three sources: long term stability, environmentally induced frequency shifts, and short term frequency fluctuations. Each of these sources is caused by different physical phenomenon. Understanding how jitter relates to frequency stability provides a better understanding of jitter and how it limits the receiver's ability to reconstruct an undersampled signal. Only when this relationship is understood can a mathematical model of jitter be used in receiver design.

Long term frequency stability refers to oscillator frequency drift over days, months, or years. The quartz resonator's aging process causes this phenomenon. For example, a crystal's elasticity coefficient changes over time, causing the quartz's piezoelectric properties to change. Therefore, the voltage produced by the quartz will change over time. The oscillator's parts per million (ppm) spec expresses the degree to which an oscillator exhibits long term frequency stability. Figure 71 shows the fractional frequency change of an oscillator over time. Figure 72 is a useful conversion chart when looking up an oscillator's long term frequency stability.

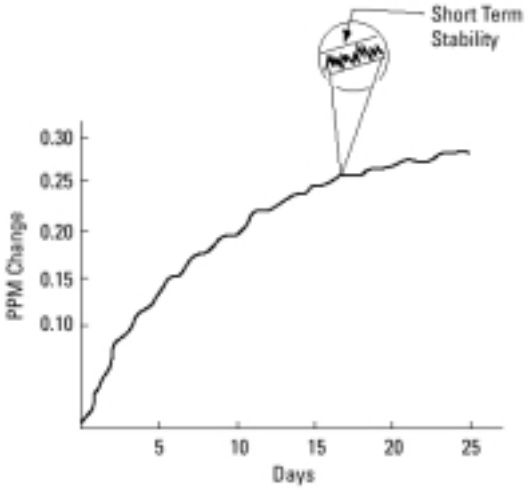


Figure 71. Long term (ppm) and short term (jitter) fractional frequency stability [68].

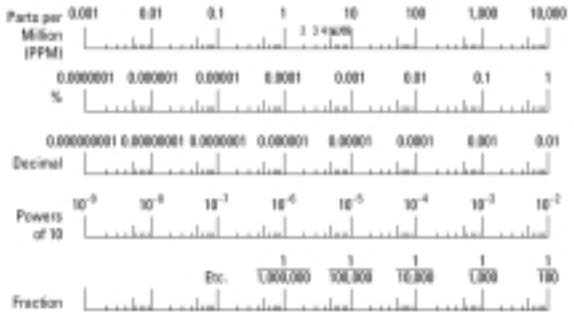


Figure 72. Useful conversion chart when looking up oscillator's long term stability [68].

The second frequency stability source is environmentally induced frequency shifts. A comparison of the damage to the frequency stability due to different environmental conditions is shown

[19] While this design didn't consider temperature compensated oscillators, a future revision should. [68] explains the different choices for temperature compensated oscillators and their function.

in Figure 73. The dotted line represents the expected frequency shift caused by a quartz resonator's natural aging process over time. These can include[68]:

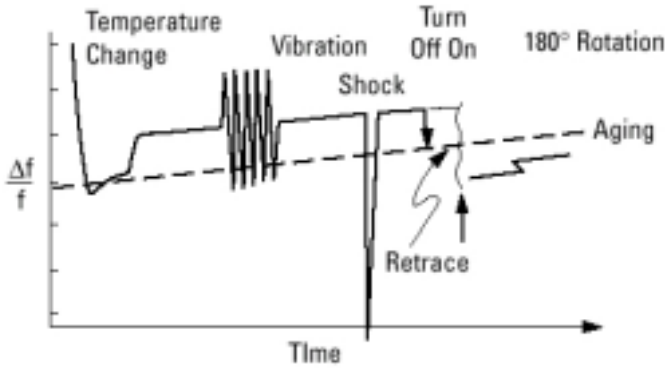


Figure 73. Environmental effects on fractional frequency stability.

- Drive Energy. Excessive drive energy levels can cause the mechanical vibrations to exceed the quartz's elastic limits, resulting in a fracture.
- Gravity. The Earth's gravitational forces can cause the physical orientation of the crystal oscillator to shift, changing the frequency.
- Shock. Striking a crystal can deform the quartz resonator's mounting structure, Figure 69, changing the frequency.
- Electromagnetism. Placing an oscillator physically close to devices that produce electromagnetic interference (EMI) can cause the oscillator's output frequency to change. This change is a result of EMI coupling into the circuitry surrounding the oscillator and changing the feedback loop.
- Retrace. Repetitive calibration of an oscillator will cause an offset in the natural aging process's trajectory over time.

The last source of frequency stability, short term frequency fluctuations, is the most critical for software radios. Since software radios undersample the signal, small variations in these sampling points over time directly effect the receiver's ability to reconstruct the data that was transmitted. The importance of this source of frequency stability for this project warrants its own section.

7.1.3 Mathematically Defining Jitter

Jitter, or clock edge variation in time, is a measurement of short term rms frequency variations, also referred to as time domain stability. The International Telecommunication Union defines jitter as "a short term variation of the significant instants of a digital signal from their ideal positions in time [70]." This definition is illustrated in the time domain by Figure 62 and in the frequency domain by zooming in on Figure 71.

There are two types of clock edge variation: deterministic jitter and stochastic jitter. Deterministic jitter can be attributed to a unique source and is called pattern jitter or "flanging" [1]. The source is usually related to subharmonics that appear as multiple modes of jitter if viewed in the time domain. Pattern jitter is low-frequency and hard to measure. Stochastic jitter can only be modeled as a random variable with respect to time. This is the type of jitter that degrades the sampling accuracy of the ADC and, as a result, degrades the BER. Oscillator manufactures can express jitter in the following ways:

- In unit intervals (UIs), describing the magnitude of the jitter as a decimal fraction of one UI. Here, one UI is one cycle of the clock frequency. This cycle is called the normalized clock period.
- In degrees, describing the magnitude of jitter in units of degree where one cycle equals 360 degrees.
- In absolute time, describing the magnitude of the jitter in units of seconds, usually in picoseconds.
- As a power measurement, describing the magnitude of the jitter in units of radians or unit intervals squared. Here, intervals squared often are expressed in decibels relative to one cycle squared [1].

Jitter is often specified on an oscillator's specification sheet in terms of jitter power. For example, an oscillator might be specified as having 2σ peak-to-peak jitter, where σ stands for the rms value. See Table 4 for a comparison of jitter units. Consult [1] for an explanation of how to derive jitter from power-spectral density, or phase-noise, measurements.

Peak-to-Peak Jitter (psec) (6.43 nsec = one cycle)	Degrees (peak-to-peak, normalized)	Unit intervals (UIs) (peak-to-peak normalized)	Unit intervals (UIs) (rms units, normalized)	Jitter power (dBi)
100	5.6	0.015552	0.0022217	-53.07
200	1.2	0.003110	0.0004443	-67.05

Table 4. Comparison of jitter units [1].

7.1.4 Experimentally Measuring Jitter

Measuring jitter is difficult since jitter measured with a standard oscilloscope will just be a measure of the scope's trigger instability [1]. A true measure of jitter requires measuring the actual position of a clock edge over time, as shown in Figure 62. One technique for locating this reference edge, discriminating subsequent edges, and charting their locations over time is shown in Figure 74. This set-up locates the trigger edge by recording, for a length of time equal to the delay, the clock stream. This set up has two parameters: the length of the delay line, τ_d , and the speed and sensitivity of the oscilloscope. Graph 12 shows how the sensitivity of this measurement is a function of jitter frequency; see [1] for a complete analysis of this measuring technique.

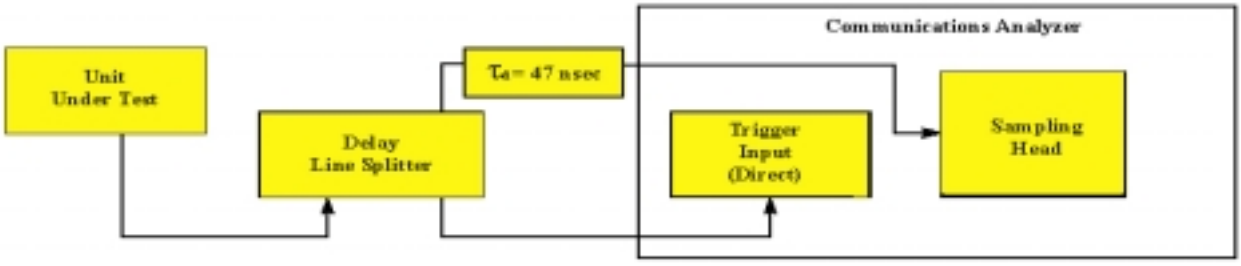
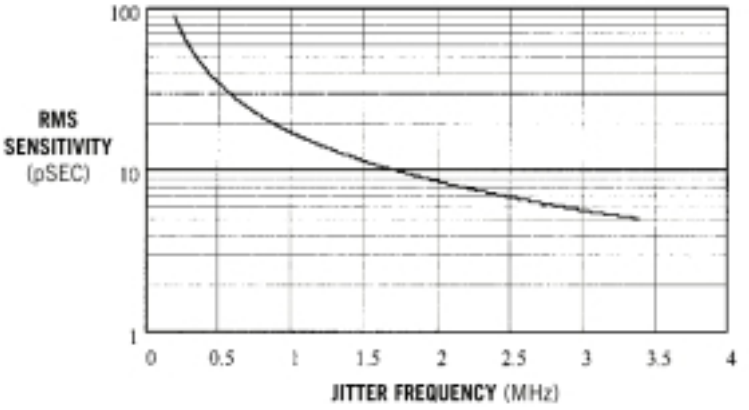


Figure 74. Using a delay line and a communications analyzer to locate the reference edge and examine the jitter on subsequent clock edges [1].

7.1.5 Effects of Jitter



Graph 12. 47 nsec delay line jitter sensitivity [1].

Sampling clock jitter causes aperture uncertainty. Aperture uncertainty can have three effects on sample-to-sample variation during the encoding process: an increase in system noise, uncertainty in the actual phase of the sampled signal, and inter-symbol interference (ISI). The effect of sampling clock jitter on the overall system phase uncertainty and ISI is minor compared to the effect it has on the overall system noise. The discussion of these effects will be three fold: a visual image of the effect of jitter on noise voltages, an analysis of how jitter degrades the noise floor, and a discussion of how jitter ultimately effects the ADC's SNR.

7.1.5.1 Noise Voltage

Figure 76 and Figure 75 show the effects of aperture uncertainty (also called phase jitter) combined with input slew rate on the ADC's internal sample-and-hold clock. This phase jitter causes a voltage error, which is a function of slew rate. The more the input signal "slews", the larger the jitter induced error voltage is created. Equation (7.1) provides a method for calculating the error voltage,

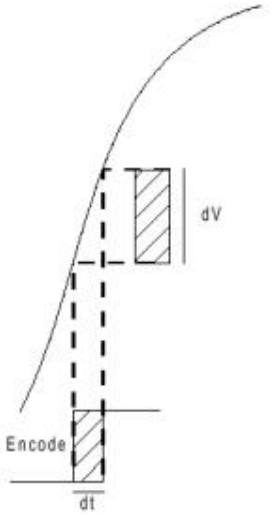


Figure 75. Diagram to help understand aperture uncertainty calculation [9].

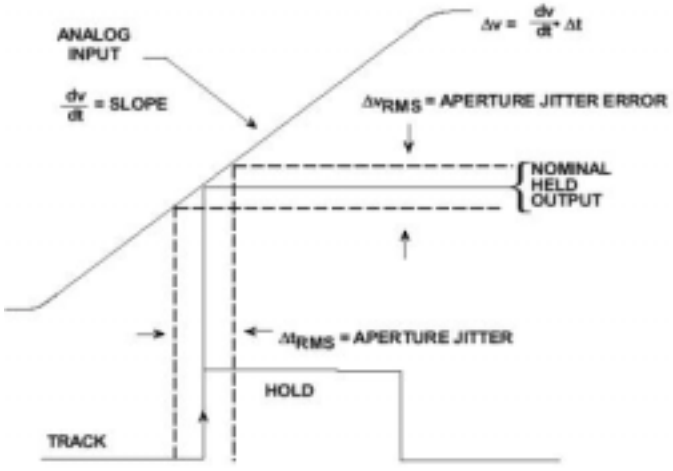


Figure 76. The effects of aperture and sampling clock jitter [8, see pg. 4-28].

V_{error}, caused by the sampling clock's aperture uncertainty, t_{jitter}, and by the input's slew rate, Slew_Rate. This voltage error results in an overall degradation in SNR.

$$V_{error} := (Slew\_Rate) \cdot (t_{jitter}) \quad \textbf{(7.1)}$$

7.1.5.2 Noise Floor

An input signal sampled by the ADC can be thought of mathematically as a multiplication of the input signal with the sampling clock[20]. Since multiplication in the time domain translates to convolution in the frequency domain, the spectrum of the sampling clock is convolved with the spectrum of the input signal. Therefore, any noise in the sampling clock's spectrum will show up on the spectrum of the ADC's output. Since aperture jitter is wideband noise, it degrades the noise floor performance of the ADC [71].

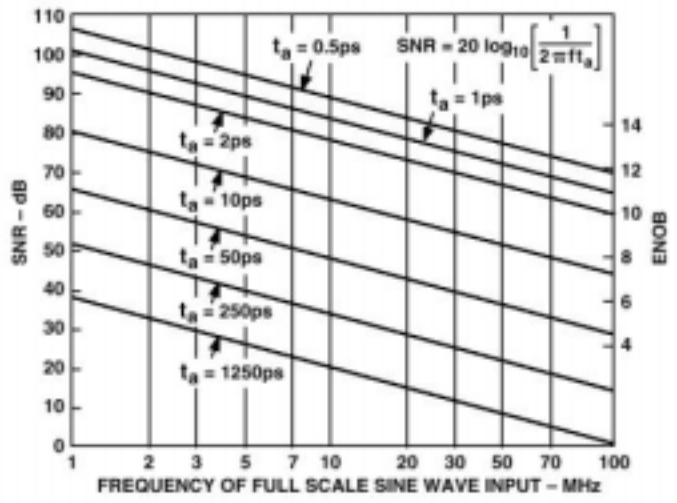
7.1.5.3 SNR

Theoretically, the ADC's SNR is limited by encoded source (the sampling clock's) jitter, differential nonlinearity, and thermal noise. Equation (7.2) is the generalized equation for SNR that can be used for system performance calculations where f_{IF} is the analog IF frequency, t_{jitter_rms} is the encode source jitter, ε is the average dnl of the converter (~0.4 LSB), V_{noise_rms} is the thermal noise in LSBs, and N is the number of bits [71]. For calculations of just the ADC, only the encode source jitter needs to be considered; see Equation(7.3). These equations provide insight into the noise performance that can be expected of a data converter.

Graph 13 illustrates the relationship between SNR, jitter and effective number of bits (ENOB). Equation (7.3) provides a method for calculating theoretical upper bound on the ADC's SNR limited by the sampling clock's aperture uncertainty [7]. In this equation, f_{IF} is the frequency of the incoming signal, t_{jitter_rms} is the jitter of the sampling clock. Therefore systems that want to sample close to the antenna, requiring a large dynamic range on the ADC, require very low jitter sampling clocks.

$$SNR := \sqrt{-20 \cdot \log\left[\left(2 \cdot \pi \cdot f_{IF} \cdot t_{jitter\_rms}\right)^2 + \left(\frac{1+\varepsilon}{2^N}\right)^2 + \left(\frac{V_{noise\_rms}}{2^N}\right)^2 \right]} \quad \textbf{(7.2)}$$

[20] The ADC can be compared to a mixer where the sampling clock for the ADC is a local oscillator and the input signal is an RF signal. Using this comparison, it is easy to see parallels between the frequency accuracy constraints on the mixer's local oscillator (a VCO in a PLL) and the jitter constraints on the ADC's local oscillator (sampling clock).



Graph 13. SNR due to aperture and sampling clock jitter [71].

$$SNR_{ADC} < -20 \cdot \log\left(2 \cdot \pi \cdot f_{IF} \cdot t_{jitter\_rms}\right) \quad \textbf{(7.3)}$$

7.1.6 Calculating Jitter for this Project

Solving Equation (7.3) for t_{jitter_rms} produces Equation (7.4). This equation sets an upper bound on the allowable jitter on the encode clock. Theoretically, the ADC will not be able to produce a SNR better than Equation 7.3 if the encode clocks jitter is more than this upper bound.

For example, in order to implement the demodulator outlined in [28], a SNR of 72 dB is required. If we assume that this means the ADC's SNR must be at least this amount, then we can determine the upper bound on the sampling clock's jitter. For an f_{IF} of 140 MHz, Equation 7.4 determines that the maximum allowable jitter on the sampling clock is 0.286 psec. Theoretically, this will limit the ADC's performance to only producing a SNR of 72 dB. Unfortunately, obtaining a clock with jitter less than or equal to this amount is nearly impossible. And an encode clock with 1 psec jitter will theoretically prevent the ADC from performing thus preventing the demodulator from getting the signal with the proper SNR needed to produce its guaranteed BER. Therefore, the SNR specification must be relaxed in order to use a commercially available clock source.

$$t_{jitter} < \frac{10^{\frac{-SNR}{20}}}{2 \cdot \pi \cdot f_{IF}} \quad \textbf{(7.4)}$$

The following lead times demonstrate how the purchase of a low jitter clock is currently a serious limiting factor in the design of SDR. Conner-Winfield will manufacture custom clocks with less than 1 ps jitter when measured over a bandwidth of 12 kHz to 20 MHz, but they have a 30 week lead time. Valpey-Fisher has 10 ps jitter clocks but a lead time greater than 30 weeks. MF Electronics has a 20 week lead time on their semi-low jitter clocks and are not able to speculate a lead time for low jitter clocks[21].

With great perseverance, six samples of a low jitter crystal oscillator were obtained from VITE Technology Express, (previously Vectron International). These crystal oscillators have the following specifications:

- 38 ps maximum jitter
- 5 V
- fixed frequency with tri-state capability
- +/- 100ppm, frequency stability
- -40 to +85 temperature
- symmetric output of 50 +/- 5% CMOS, 15pF
- 20 weeks lead time for VCC1
- CCTH = old labeling, VITE = new labeling

7.1.7 Jitter's Effect on System Performance

The final objective of the base station is to discern a 1 or a 0 from the received RF signal. The last step in the process is quantization. At this step, the FPGA or DSP determines if the digitized waveform is a 1 or a 0 at a particular time. A critical factor is determining when the FPGA or DSP should "look" at the waveform. The optimum time to "look" is at the center of each transmitted clock cycle. Determining if a waveform is a 1 or a 0 at a particular point in time is much easier when the waveform resembles Figure 77, but becomes progressively more difficult for Figure 78, and is nearly impossible for Figure 79. These figures illustrate the idea of how an eye diagram can "collapse." An eye diagram is simply the cumulative graphical portrait of the edge placement. When the sampling clock's edge varies in time, the edge of the ADC's output will vary in time. An edge that varies over time will

[21] Interesting side note: the sales representative, after carefully taking down the specification for my request, laughed when I asked if the clock could be FedEx'ed ASAP. She told me she could FedEx them to me *any time next year*. Then I asked to talk to a technician and he told me that he could pay off the mortgage on his house by standing at the street corner and offering to sell low jitter crystal. He then explained how the mining of the quartz is the limiting factor world-wide.

make the resolution between bytes fuzzy; this phenomenon is called “collapsing the eye”. Sampling clock jitter is a dominant source for the collapsing eye diagram.

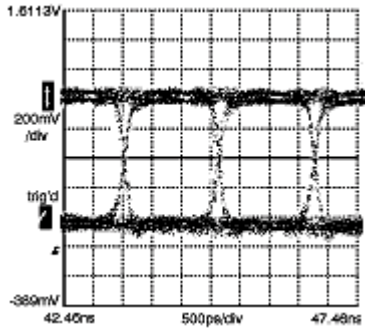


Figure 77. Eye diagram with no jitter [69].

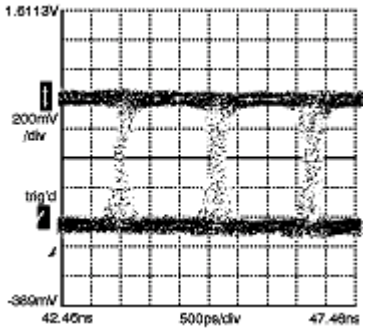


Figure 78. Effects of medium amounts of jitter [69].

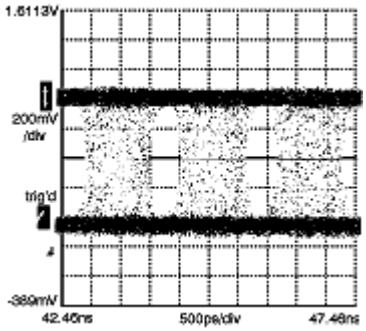


Figure 79. Effects of high levels of jitter [69].

8 Digitizing the Signal

8.1 ADC

The AD6600's ability to sample up to 20 MSPS, take in an IF frequency up to 250 MHz, and provide 90+ dB signal range made it an ideal choice for this application. Figure 80 shows a functional block diagram of the ADC's capabilities.

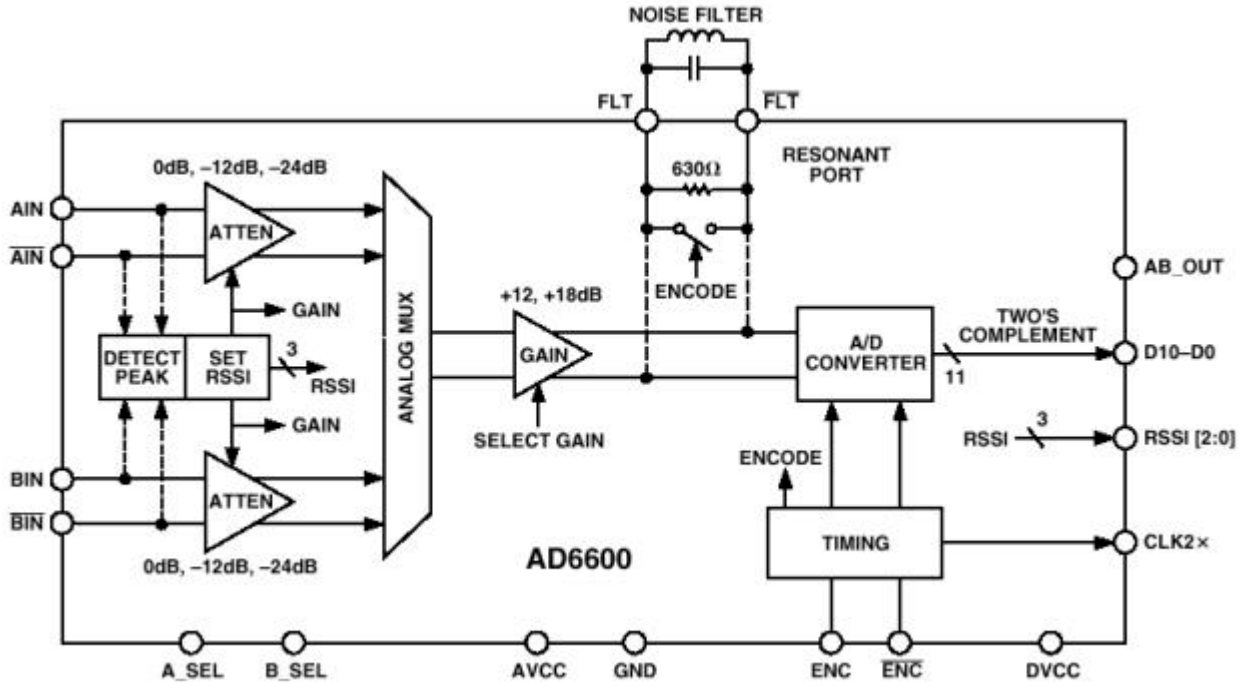


Figure 80. Functional block diagram of the ADC [72].

The bad side of any ADC is the noise sources induced just by the very act of sampling. The ramifications of some of the noise sources diagrammed in Figure 81 had to be determined and compensated. The most critical noise source for software radios is sampling clock jitter, discussed in the previous section. Another critical question is the amount of quantization noise. Quantization noise raises the noise floor, reduces the SNR, and increases the BER. The higher the oversampling ratio (the ratio of sampling frequency to channel bandwidth see Graph 14), the more the quantization noise is spread into a wider spectrum. Spreading it into a wider spectrum makes it easier for the digital LPF to remove it, thus improving the SNR and reducing the effective BER. Figure 82 illustrates this phenomenon.

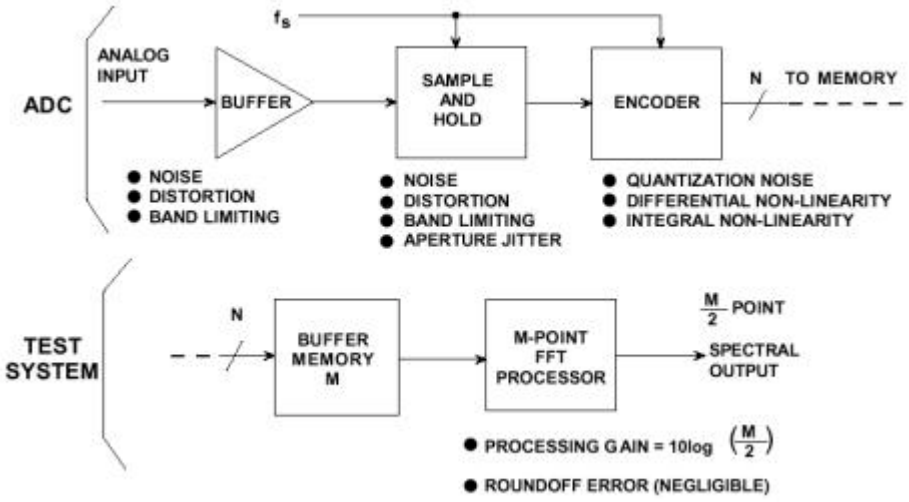
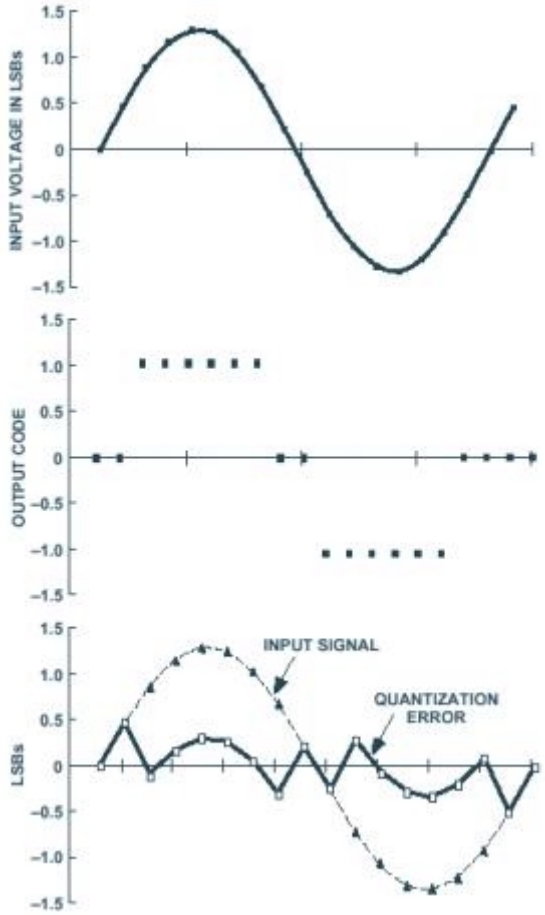


Figure 81. ADC model showing noise and distortion sources [8, see pg 4-14].



Graph 14. An illustration of quantization noise an d square waves and dithering [73].

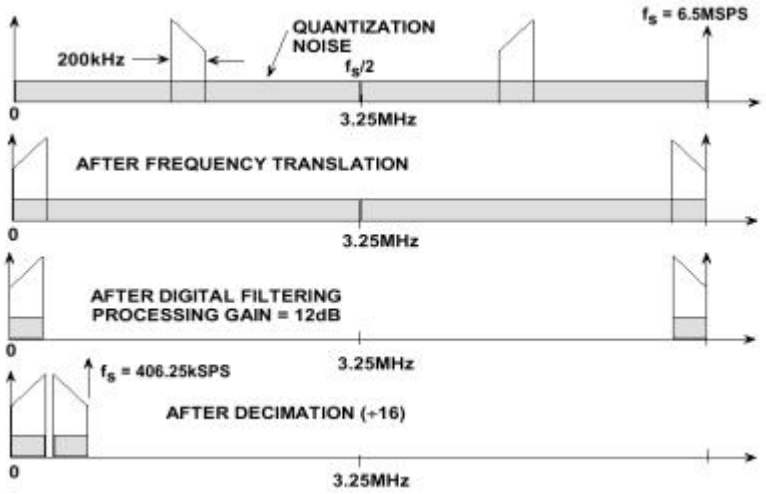


Figure 82. digital filtering and decimation example [74, see pg 5-29].

8.2 Timing

Once the ADC and the LPF are chosen and the sampling clock's jitter is determined, the timing between all the digital components must be calculated. The signal path is as follows: the ADC's outputs are buffered, sent to the digital board via twisted pair cables, latched into the digital board, and are fed to the LPF. The buffers and latches ensure that the signal remains intact as it travels from the ADC to the digital signal processing chips.

Two decisions must be made: the frequency at which to run the LPF and the delay needed between the clock edges of the digital components. Since the ADC and the LPF need to be synchronized, the options for the first decision are restricted to either the same clock as the ADC or the clock generated by the ADC from the sampling clock. As illustrated in Figure 80, the ADC takes in the low jitter clock, called the encode (ENC) signal, and produces twice the ENC. Therefore, the Digital LPF can be run at either ENC, the sampling clock's rate, or 2xENC, twice the sampling clock's rate.

The more computations per input sample the LPF can do, the better. Therefore, as long as the set-up and hold times can be met, and the LPFs processor speed can take it, running the LPF at 2xENC will produce the best BER. This design runs the ADC at ENC (16 MHz) and the LPF at 2xENC (32 MHz). Since the buffers and latches are there to ensure the digitized signal makes it to the LPF's input, they are clocked at the same rate as the ADC.

Now that the clocking rates are chosen, the next task is to figure out the timing between these clocks and the signals of interest. Figure 83 and Figure 84 illustrate the timing parameters and options that can and need to be determined. Each device has a minimum and maximum propagation delay. A

timing diagram is drawn to ensure every signal, traveling from the ADC to the LPF, meet the set-up and hold times. Instead of checking every path through the circuit, it is sufficient to just check the best and worst case scenarios, as done in Figure 85. First, this timing diagram verified that the slowest signal, the one that experiences the longest propagation delays, still meets each part's set-up time. In addition, the diagram verified that the fastest signal, the one that experiences the shortest propagation delays, still meets each part's hold-time. This verifies that the signals traveling from the ADC to the LPF are valid when the part is clocked.

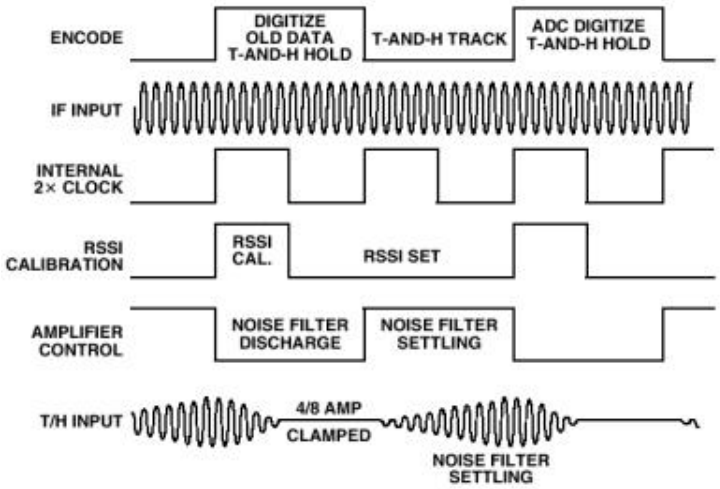


Figure 83. AD6600: ADC's internal timing [72].

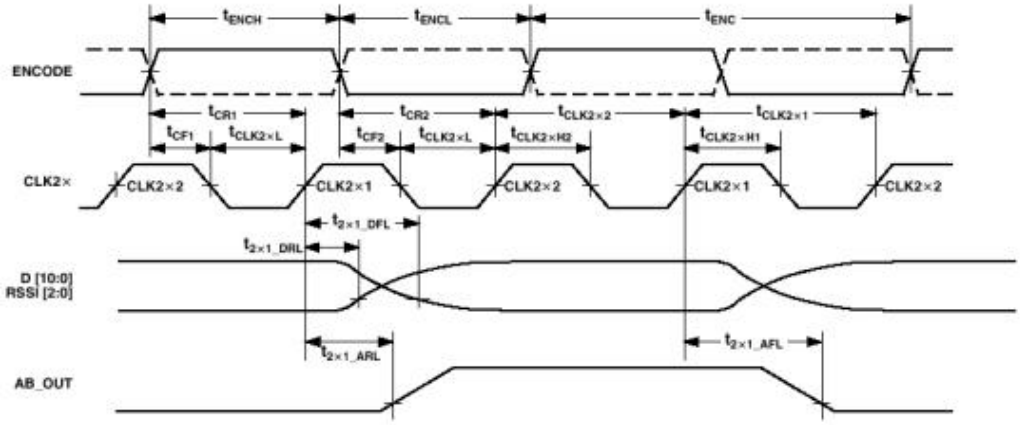


Figure 84. AD6600 timing diagram: encode to CLK2x delays and CLK2x propagation delays [72].

The worst case and the best case scenarios were examined with the buffers and latches being clocked with different amounts of delay. A NAND gate is to used produce different delayed copies of the ENC and 2xENC, as illustrated in Appendix B :Schematic. One NAND gate has a propagation delay of 1.5-9 ns. After a careful analysis of the timing options available, the following results, listed in Table 5, allowed both the worst and best case scenarios to meet all the set up and hold time constraints. Figure 86 is a quick block diagram sketch illustrating the timing parameters between the RF and digital board.

Part	**Clock**		**Delay** (min, typ, max)	
ADC	ENC	16 MHz	0	0
Buffer	ENC	16 MHz	$2*t_{p\_NAND}$	3.5, 12.5, 17.5 ns
Latch	ENC	16 MHz	$2*t_{p\_NAND}$	3.5, 12.5, 17.5 ns
LPF	2*ENC	32 MHz	$t_{p\_CRI+2tp\_NAND}$	25.652, 36.125, 42.625 ns

Table 5. Results of timing analysis.

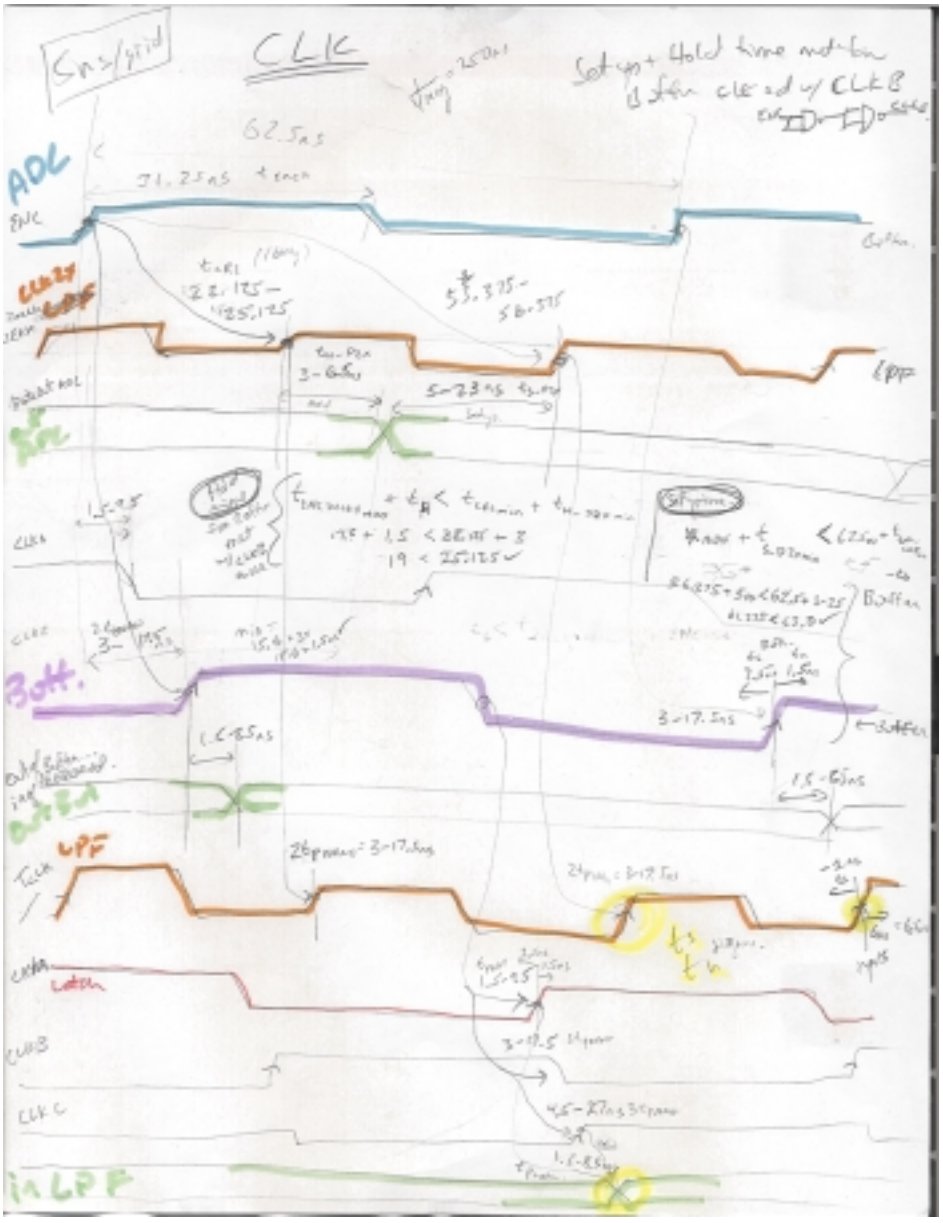


Figure 85. A quick sketch illustrating the number of timing constraints that had to be considered.

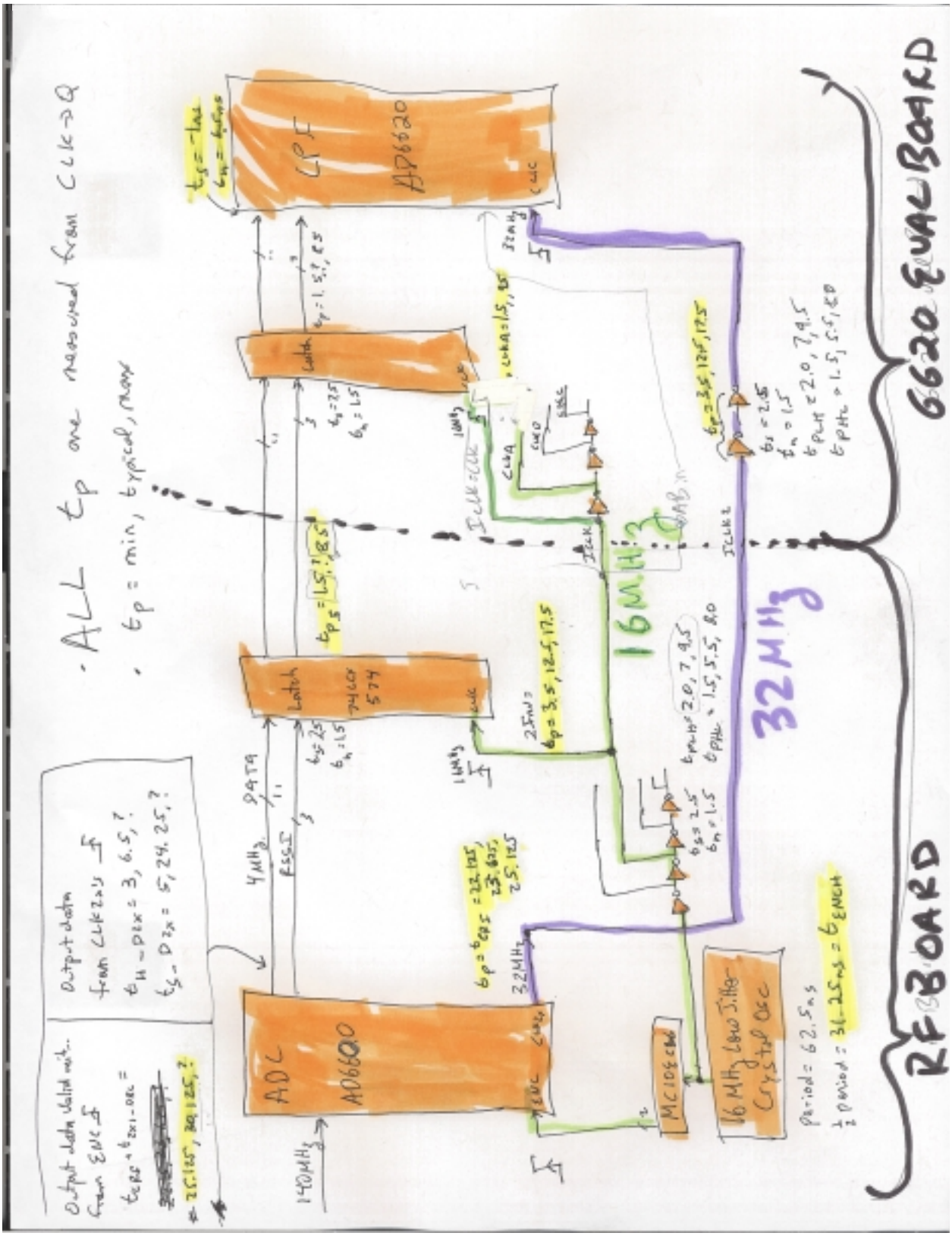


Figure 86. Quick block diagram sketch illustrating results of the timing analysis.

8.3 Signal Processing

After leaving the RF board, the digitized signals are latched into digital board containing a digital LPF and an FPGA. The digital LPF performs frequency decimation and filtering. Then the FPGA recovers a clock and finally demodulates the GFSK signal and recovers the bits. The processor speed and size are bottleneck for IF signal processing [3].

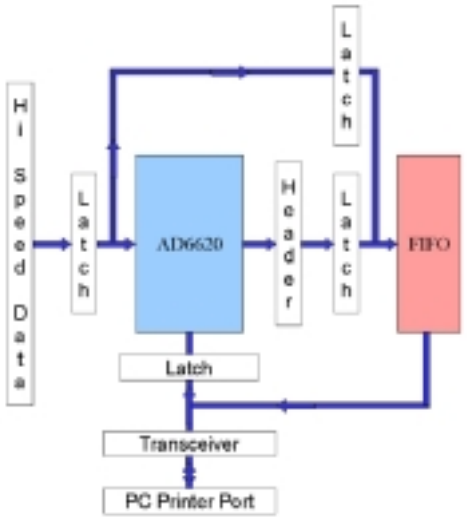


Figure 87. Block diagram of the AD6620 evaluation board [75].

8.3.1 Digital LPF

Once the signal has met the necessary set-up and hold times, it must go through a decimating low pass filter to remove unwanted noise and frequency shift the signal, making baseband processing easier. This design uses Analog Device's 6620 digital LPF [76]. Figure 88 illustrates the device's four cascaded signal processing elements: a frequency translator, two fixed coefficient decimating filters, and a programmable coefficient decimating filter. The header for this project's RF board is designed to mate with the 6620 Evaluation Board, as shown in Figure 87. Therefore, the 6620 software, Figure 89 and Figure 90, can be used determine the which LPF parameters produce the best BER for a given transmitter. The 6620 evaluation board manual [75] and the application note "Designing Filters with the AD6620" [77] assists in determining these LPF parameters.

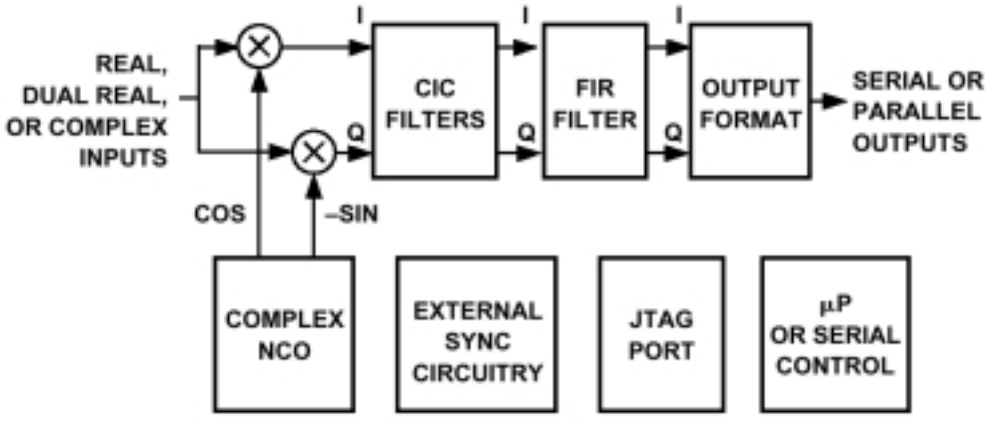
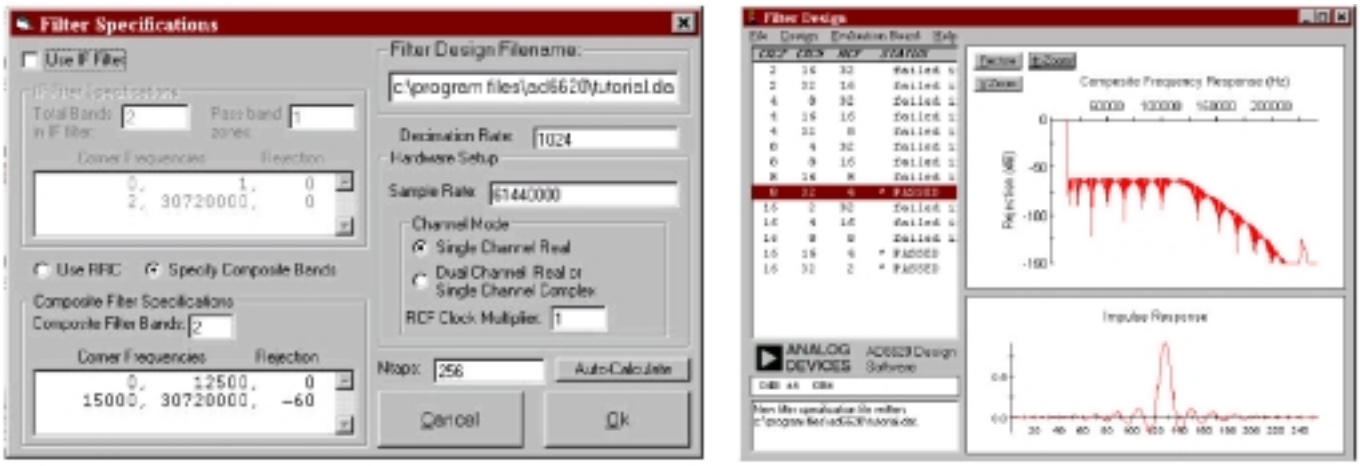


Figure 88. Functional block diagram of the AD6620, with four cascaded signal processing elements: a frequency translator, two fixed coefficient decimating filters, and a programmable coefficient decimating filter [76].



(a) Filter specification program **(b) Filter design program**

Figure 89. AD6620 evaluation board's software for filter specification and design [78].

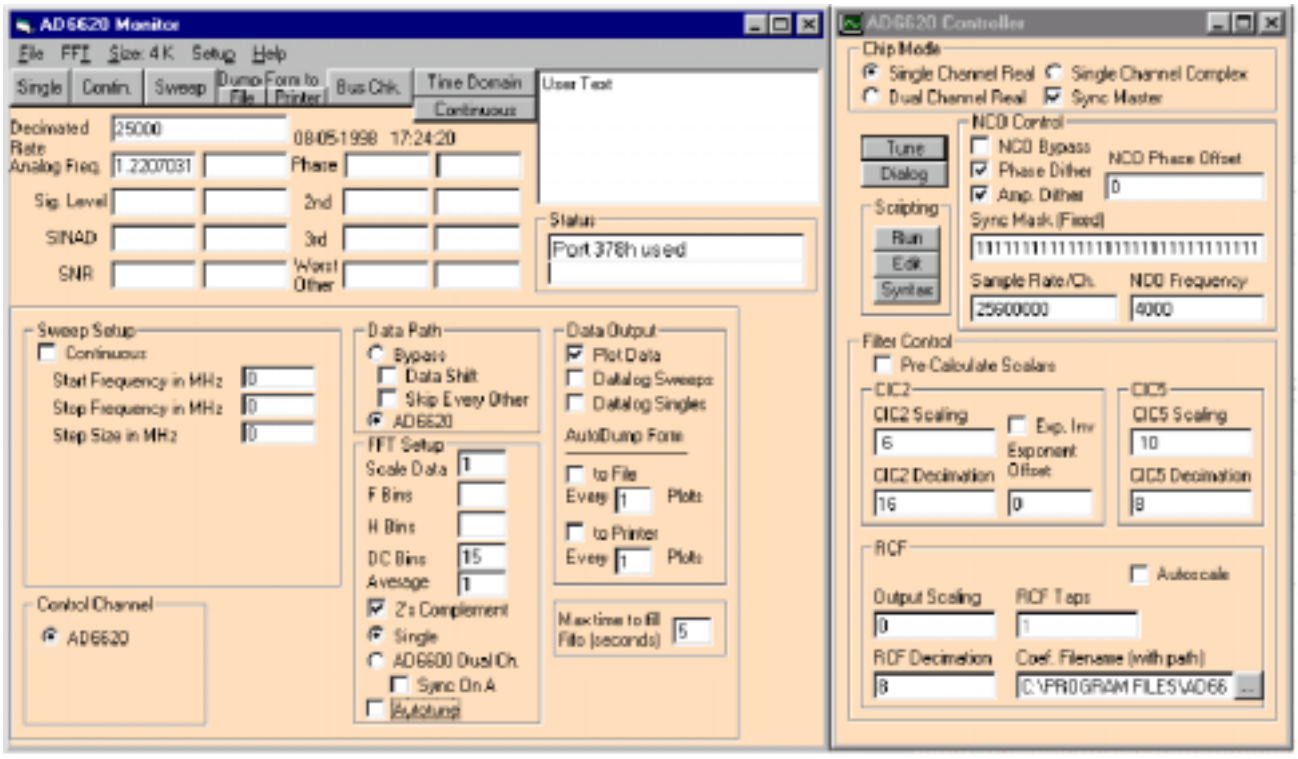


Figure 90. AD6620 evaluation board's control program [75].

8.3.2 Clock Recovery

After passing through the digital LPF, the signal enters an FPGA. Here clock recovery and demodulation are performed. Clock recovery, also called clock extraction, is the process where the receiver determines when, in time, to "look" at the incoming data. The edges of the recovered clock determine when the FPGA will quantize the data, decide if the digitized waveform at that instant in time is a "1" or a "0." There are many ways to perform clock recovery. The following papers present different clock recovery techniques: [79, 80]. Size restrictions in the FPGA determine which implementation is feasible.

8.3.3 Demodulation

Once a clock has been recovered from the signal, demodulation of the GFSK signal can occur. The goal of demodulation, or detection, is to extract the original baseband signal with minimum distortion, noise, intersymbol interference (ISI), etc. Since "frequency demodulation can be performed, in principle, by any circuit whose transfer function is sensitive to frequency [43]", there are a multitude of choices of demodulators. In this design, the size constraint of the FPGA limits which GFSK demodulators can be implemented. The following papers illustrate different demodulators optimized for IF sampling receivers: [81-85].

8.4 Power and Ground

This system has two boards: one noisy power and ground plane for the digital boards and one, hopefully, quiet power and ground plane for the RF and analog electronics. DGND refers to the digital ground plane. AGND refers to the analog ground plane. Since great care must be taken in connecting power and ground pins to their appropriate locations, Figure 95 through Figure 93 were used as guidelines. Figure 91 illustrates the star topology concept, where the center of the star can either be the ADC or the power supply but not both. The use of ferrite beads for power supply isolation is illustrated in Figure 92. Diodes are used in Figure 93 to keep the voltage between the two ground planes minimal. Figure 94 demonstrates the importance of connecting BOTH the DGND pin and the AGND pin of the ADC to the AGND plane. (say one more sentence about this) Figure 95 illustrates how the ADCs bypass caps and ground pins must be connected to the AGND plane while the buffer's bypass caps and ground pins must be connected to the DGND plane. Appendix C: Board Layout illustrates how all of these concepts are implemented in this design.

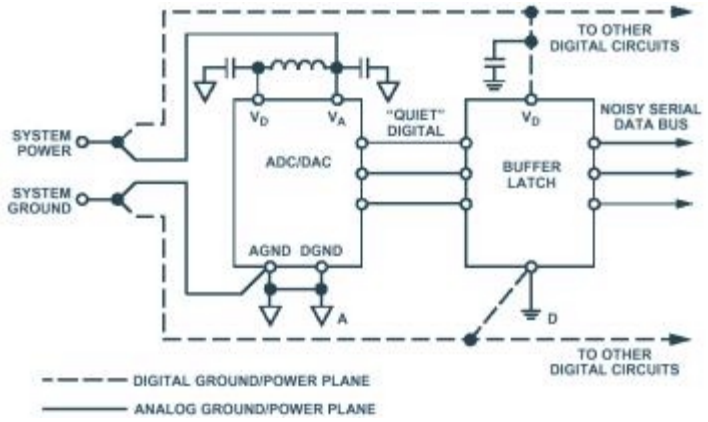


Figure 91. Separating the analog and digital grounds [86].

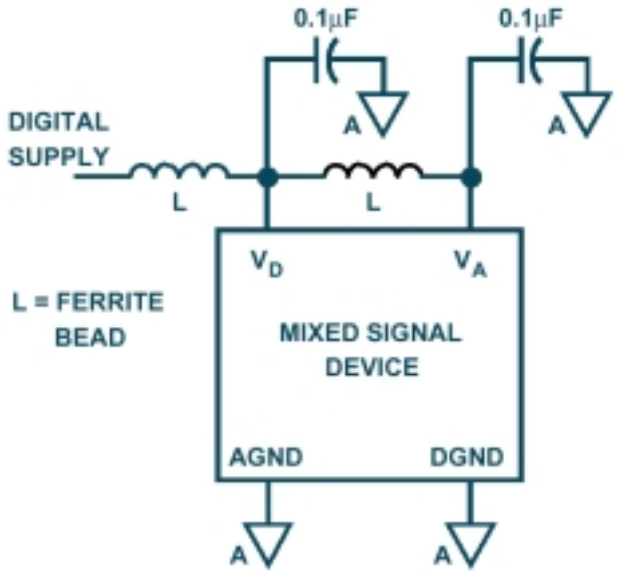


Figure 92. Use of ferrite beads to isolate power planes [87].

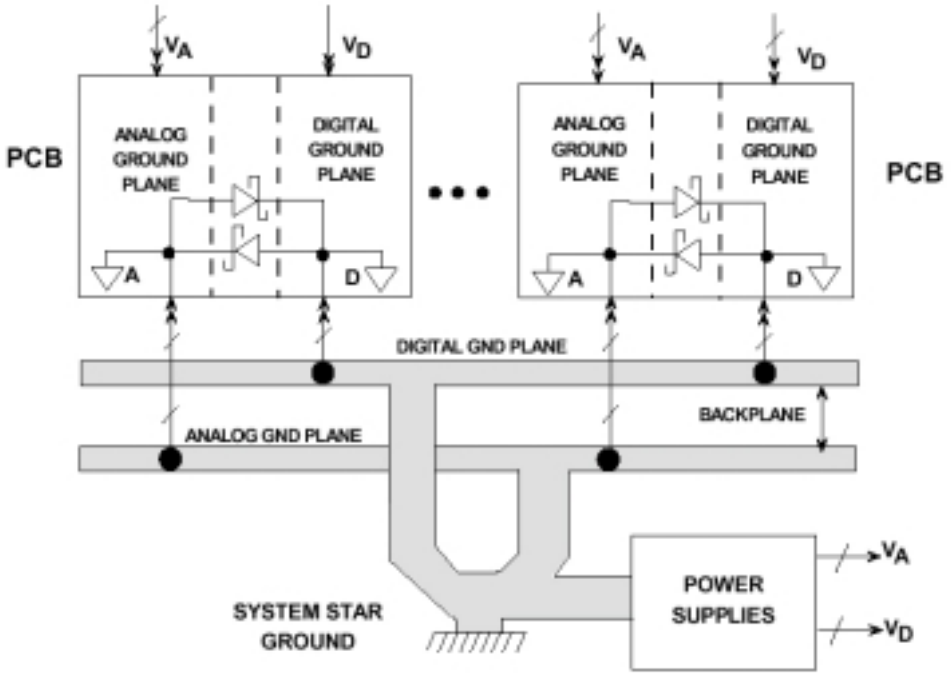


Figure 93. Using diodes to separate analog and digital ground planes.

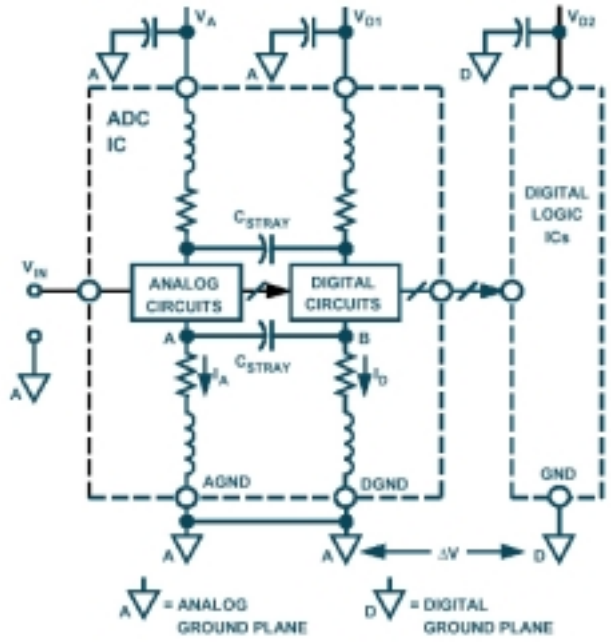


Figure 94. Grounding an ADC's digital pin on AGND plane [87].

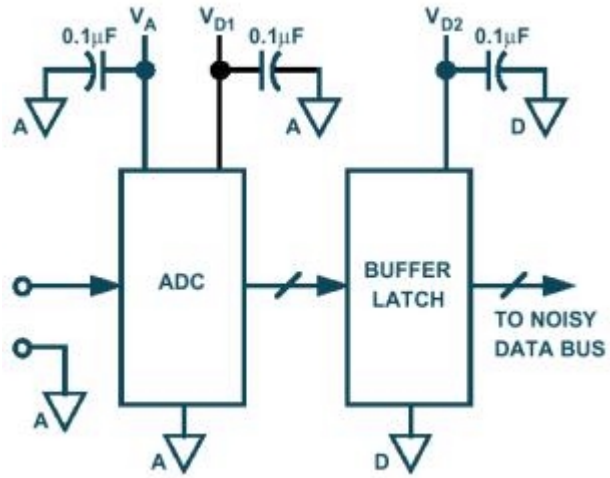


Figure 95. Buffering the outputs of the ADC to reduce noise on ADC inputs [87, pg 21].

9 Results

The system level analysis determined the noise performance and limitations for each block of the base station. Table 6 summarizes the constraints and limitations for a base station, built with commercially available parts, that is capable of producing a BER no worse than 10^{-3}, with an input signal whose received signal strength is –80 dBm or less. Table 1 summarizes the parameters for the parts that were selected for implementation. Table 7 summarizes the frequency requirements and limitations for this design.

Though the board was not debugged at the time of this write-up, the detailed design, schematics and board layout can be found in Appendix A :Block Diagram through Appendix C: Board Layout. Appendix E :Using the Testing Equipment outlines how the board will be tested and specified.

Section Name	**Parameter**	**Value**
Total System	BER	10^{-3}
Transmitted Signal	Receive Signal Strength	-80 dBm to –10 dBm
Antenna Port	Available Noise Power	-92.4 dBm
Total System	Noise Bandwidth	4.6 MHz
RF Front End	Cascaded Noise Figure	5.70 dB
RF Front End	Noise Floor	-161.6 dB
RF Front End	IIP3 Point	-9.84 dBm

Table 6. Radio performance limitations.

Name	**Value**
RF Center Frequency	= 1.890 GHz
Data Rate	= 2.5 Mbps or 1.25 Mbps
Channel Bandwidth	= 3.325 MHz (99.9% power)
GFSK's BT	= 0.5 +/- 0.05
IF Frequency	= 140 MHz
Local Oscillator's Phase Noise	< -79.4 dBm
Sampling Clock's Jitter	< 40 ps (based on oscillator availability)

Table 7. Frequency requirements.

10 Conclusions

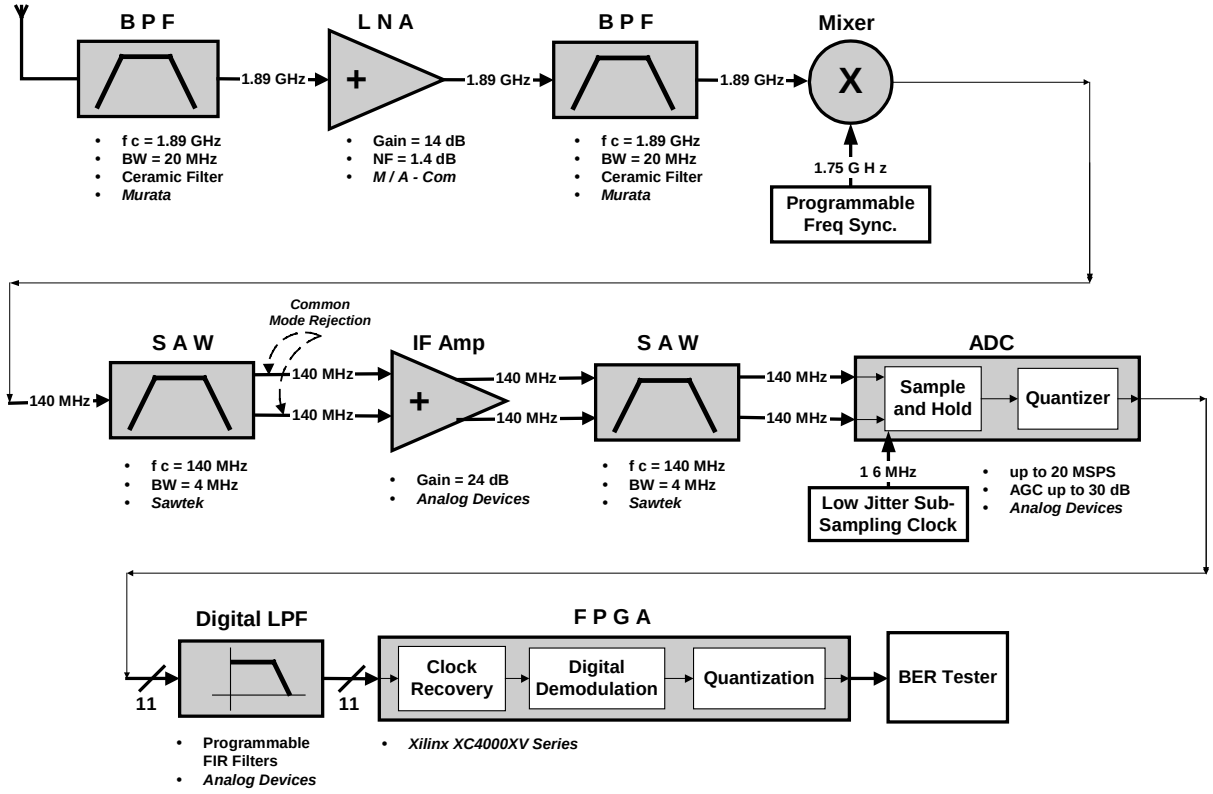
Over the past 6 years, software radio has emerged from military research to become a commercially needed strategy for affordable, ubiquitous, global communication platforms [6]. Ideal software radios, as shown in Figure 7, are actively being researched and developed although they aren't readily available. The Software Defined Radio Forum [12] is working to develop open architecture standards, to be ready for use once the ADC, DSP, FPGA, and ASIC manufacturers build the needed hardware, and once the governmental regulatory offices are ready for software radios.

This thesis examines one piece of the puzzle. It presents the theory, design trade-offs, and implementation considerations that must be addressed before building a base station. A possible design utilizing commercially available parts is recommended. The objective of this design is to create a base station that digitizes as close to the antenna as possible, given the following constraints: using commercially available chips, producing the lowest BER possible, digitizing as close to the antenna as possible, and receiving a 2.5 Mbps, GFSK modulated, 1.89 GHz signal between –80 dBm and –10 dBm.

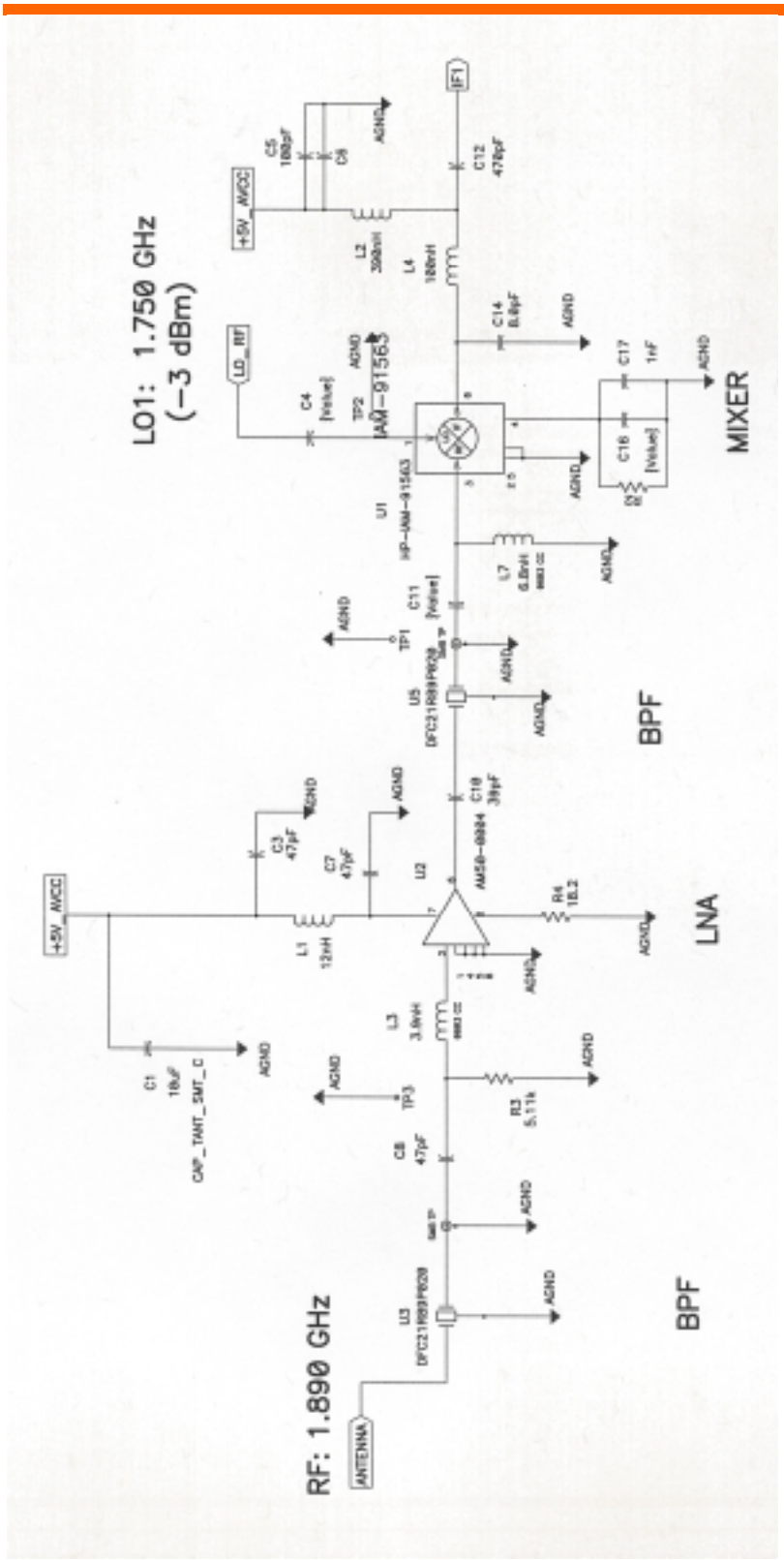
This document presents one implementation of an IF-sampling base station. The suggested design produces: a BER of 10^{-3} at –85 dBm, SFDR of 60 dB, and an IIP3 point of –9 dBm. As the performance and capabilities of the ADC and the digital signal processing chips increase, and the RF simulation tools improve, the location of the digitizing can move closer and closer toward the antenna.

Future revisions of the board could include a backchannel, multi-access capabilities, passive listening for RF signals, adaptive link equalization, and capabilities for multiple digital processing modulation schemes. Ultimately, the software radio should be able to passively listen to surrounding RF signals [88], automatically download the needed signal processing algorithms, and seamlessly operate between multiple standards. With the diligent work of researchers and scientists, soon the world will have reconfigurable, interoperable transceivers.

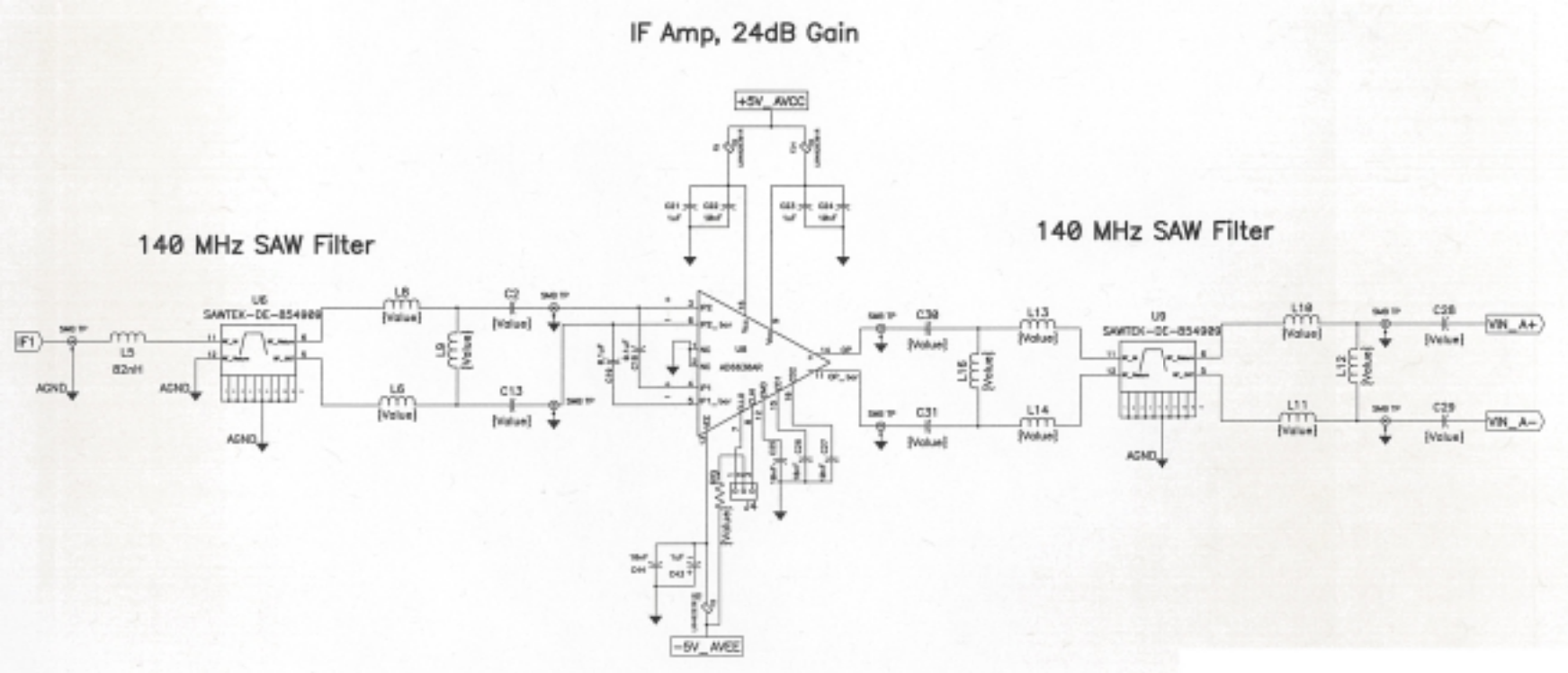
Appendix A : Block Diagram



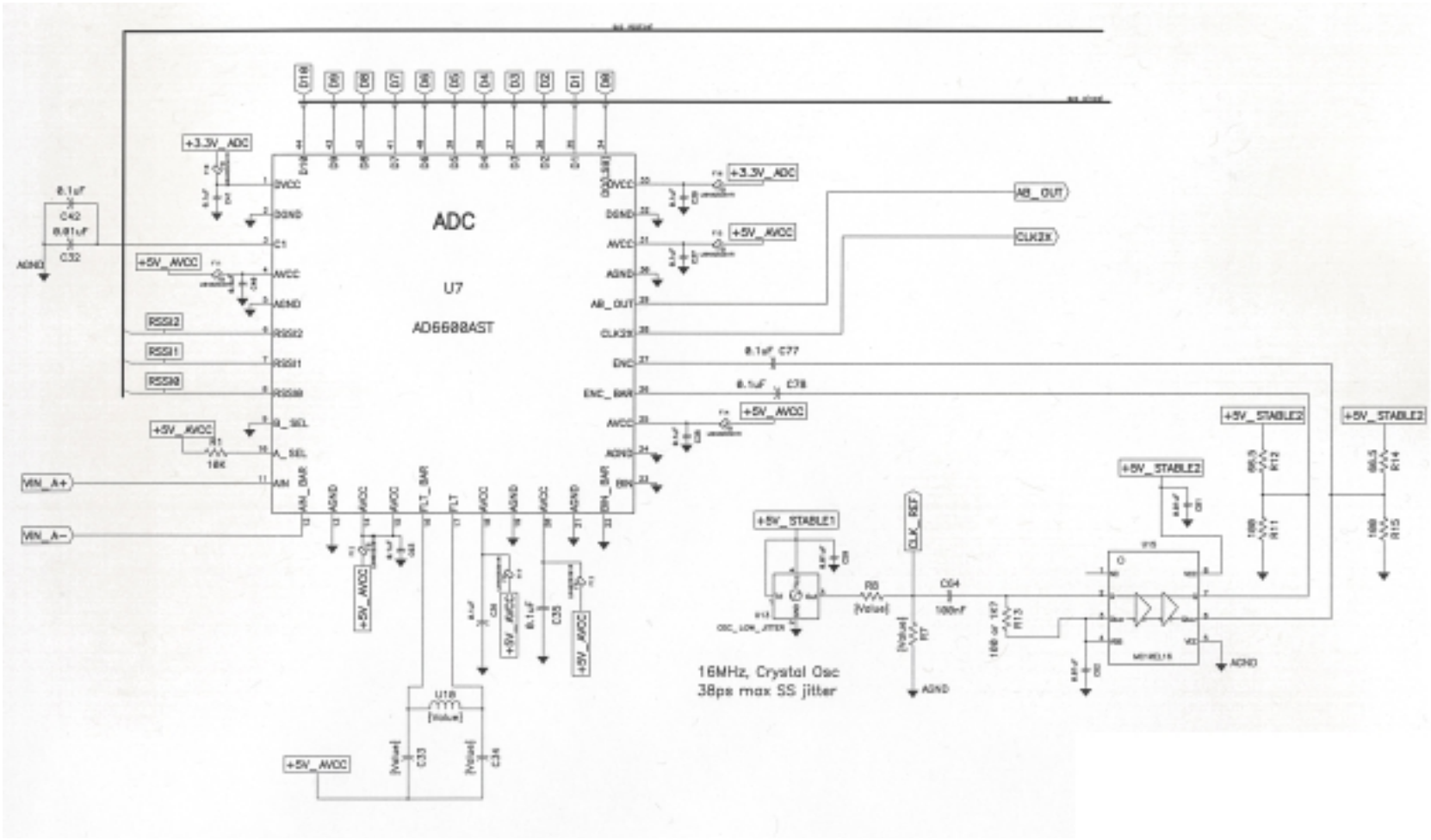
Appendix B : Schematic



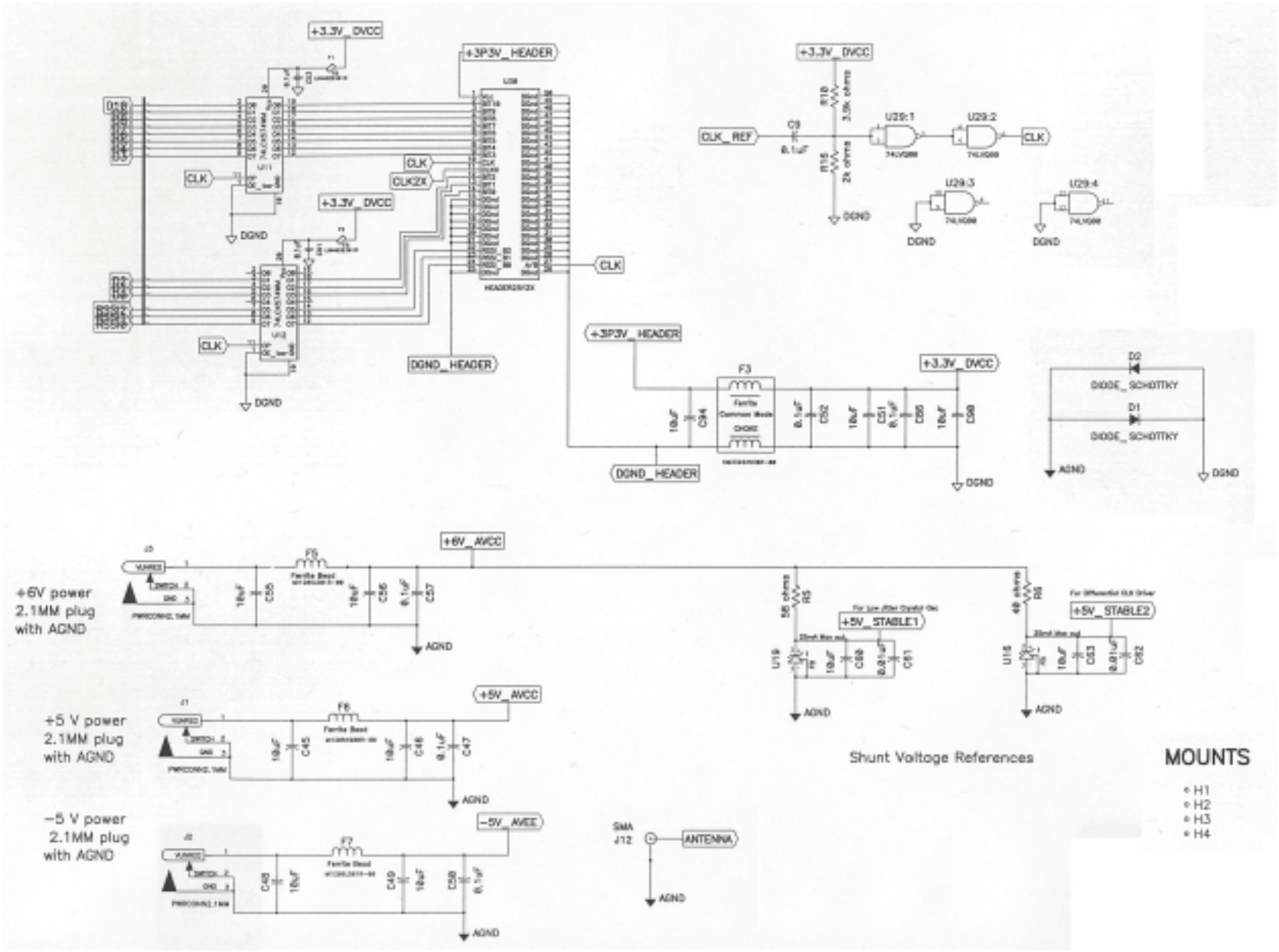
Front End and Downconverter



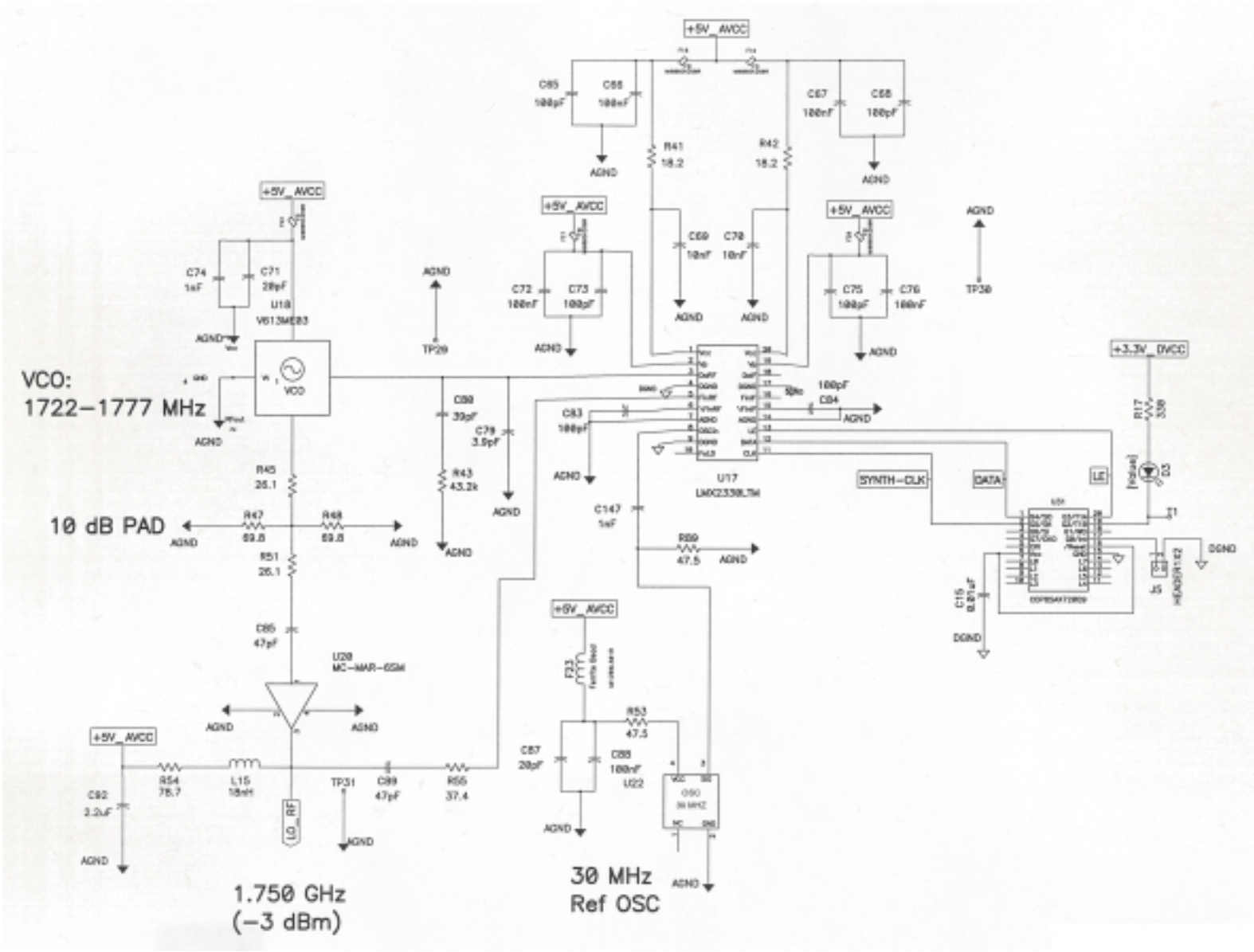
IF Filtering and Amplification



ADC and the Low Jitter Clock

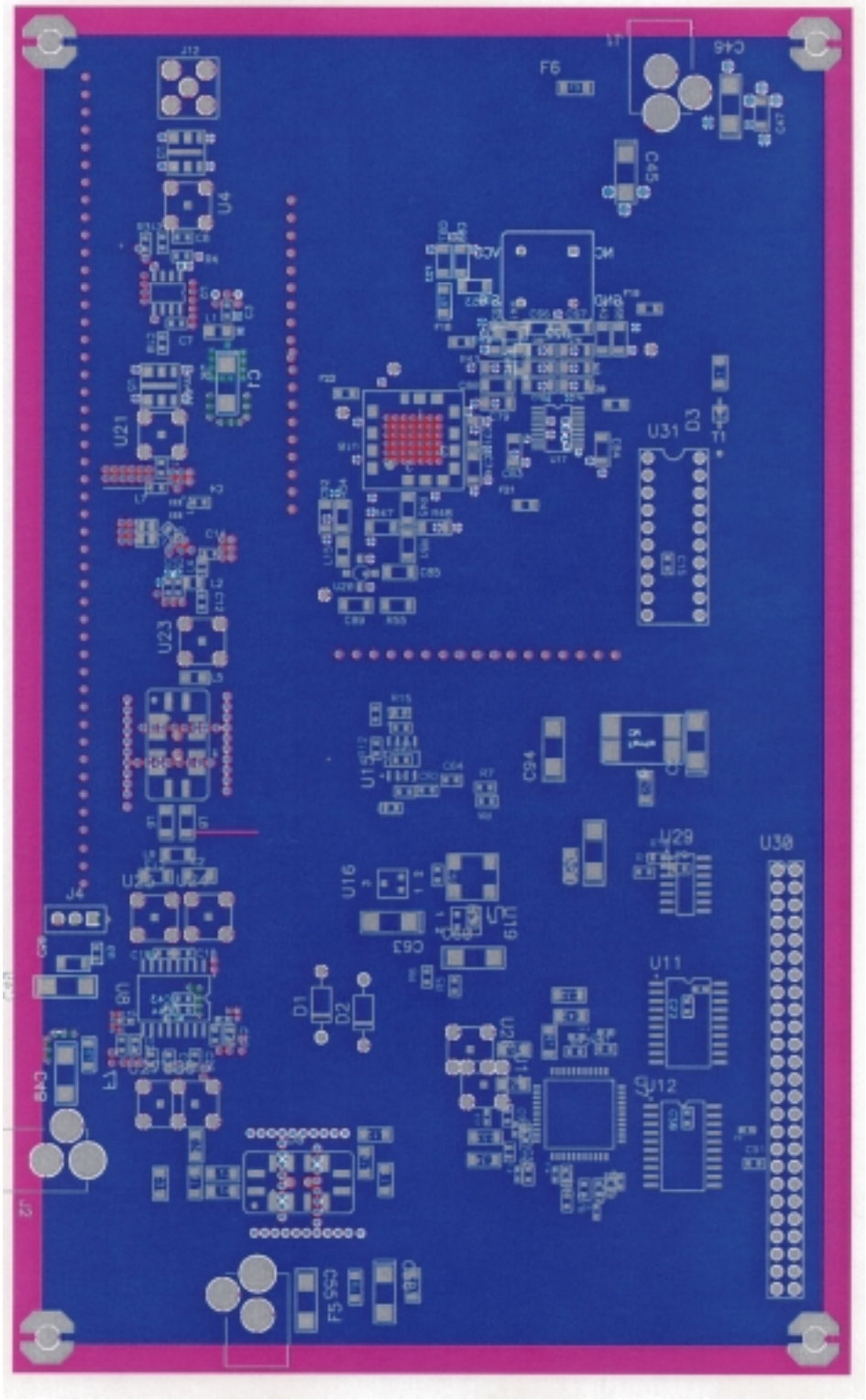


RF Board Connectors and Power Supplies



PLL: Ref. Osc., VCO, Freq. Sync. , and Microcontroller

Appendix C : Board Layout



Top, Ground, Power, Bottom Layers

Appendix D : Bill of Materials Highlights

Section	***Part Description***	***Part #***	***Manufacturer***
RF front end	**Antenna - SMA stub**	1850-1970	Centurion
RF front end	**Antenna - pico cell**	1850-1990	Smartant
RF front end	**BPF = Ceramic Filter**	DFC21R89P020HHE	Murata
RF front end	**TX/RX control**	MRFIC1801	Motorola
RF front end	**LNA**	AM50-0004	M/A-Com
RF front end	**BPF = Ceramic Filter**	DFC21R89P020HHE	Murata
Downconversion	**Mixer**	IAM-91563	HP
Downconversion	**VCO**	V613ME03	Z-Comm
Downconversion	**Amp, 50 ohm**	Mar-6SM	Mini-circuits
Downconversion	**Frequency Synthesizer**	LMX2330LTM	National
IF Filtering	**140 MHz SAW**	854909	Sawtek
IF Filtering	**IF Amp**	AD6630	Analog Devices
IF Filtering	**140 MHz SAW**	854909	Sawtek
ADC	**ADC**	AD6600	Analog Devices
ADC	**Low Jitter Clock**	VCC1-xxA-16M000, old label: CCTHLJ	Vitechnology, Vectron
ADC	**Differential Buffer**	MC10El16D	ON Semi
ADC	**Voltage Reference**	FAN4041	Fairchild
ADC	**NAND**	74LVQ00	National
ADC	**Buffers (D FF)**	74LCX574WM	Fairchild
Digital	**LPF**	AD6620	Analog Devices
Digital	**FPGA**	XL4000XL	Xilinx

Appendix E : Using the Testing Equipment

Jitter Measurements

Figure 96 illustrates the test setup recommended to measure jitter.

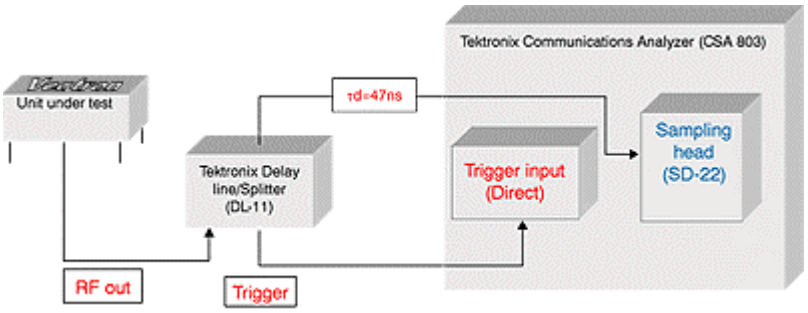


Figure 96. Testing setup recommended to measure jitter over time [69].

Phase Noise Measurement

Figure 97 illustrates the test set-up recommended to measure phase noise.

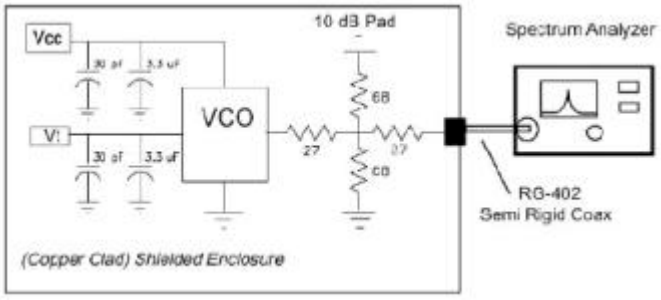


Figure 97. Phase noise measurement set-up of the VCO [89].

Trasmission/Reflection Coef, S-Parameter Test Set-up

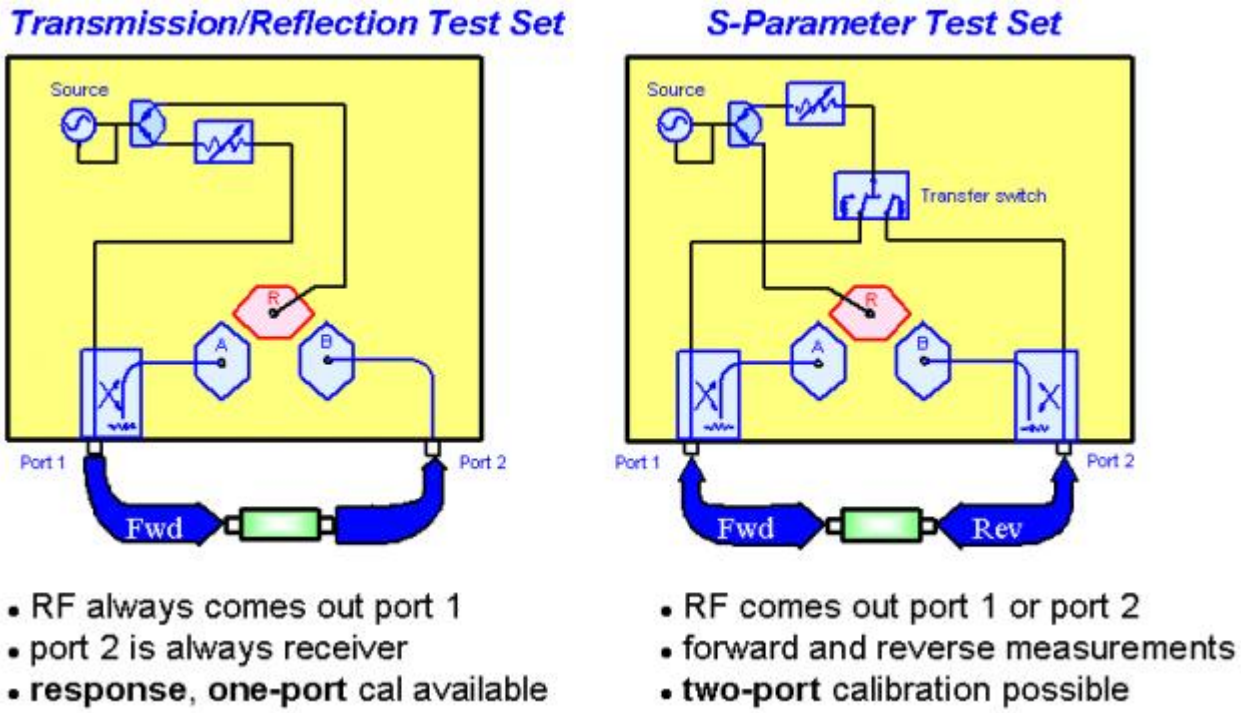


Figure 98. Transmission/reflection vs. S-parameter test set-ups [90, slide 191]

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